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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H01L 21/68, B65G 1/00, 35/00, 37/00, 41/00, 43/00, 49/07

A1

(11) International Publication Number: WO 99/17356

(43) International Publication Date: 8 April 1999 (08.04.99)

(21) International Application Number: PCT/US98/00132

(22) International Filing Date: 6 January 1998 (06.01.98)

(30) Priority Data:
08/940,524 30 September 1997 (30.09.97) US
08/990,107 15 December 1997 (15.12.97) US

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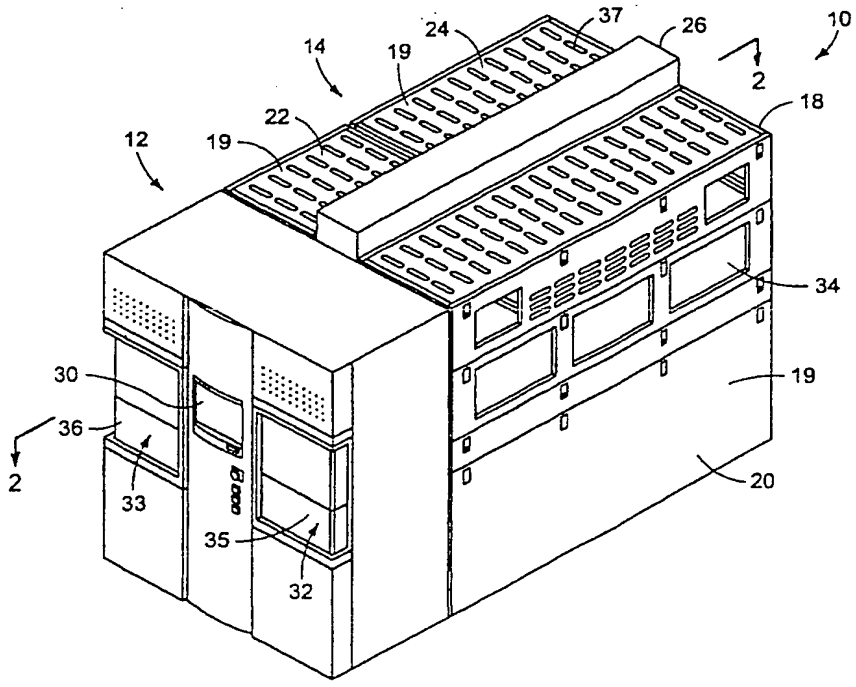
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: SEMICONDUCTOR PROCESSING APPARATUS HAVING LINEAR CONVEYOR SYSTEM

(57) Abstract

A transport system for manipulating a semiconductor wafer in a processing tool (10) is set forth. The system includes a transport unit guide (66) disposed within the processing tool (10) for supporting a wafer transfer unit (61) as the unit moves between a first position and a second position. The transport unit guide (66) comprises a frame (65), a lateral guide rail (63) mounted on the frame (65), and a series of magnetic segments (71, 74) arranged upon the transport unit guide (66) proximate the lateral guide rail (63). The wafer transfer unit (62) includes a tram (84) translatably attached to the lateral guide rail (63) and a wafer transfer arm assembly (86) for manipulating the semiconductor wafer. An electromagnet is mounted on the tram (84) in cooperative relation with the magnetic segments (71, 74) for moving the transfer unit (62) along the guide rail (63). Actuators are used for controlling the position of the transfer unit (62) and transfer arm assembly (86), and sensors (91) are used for determining the position of the transfer unit (62) and transfer arm assembly (86). A controller (101) is disposed remote of the wafer transfert unit (62) and directs the movement of the transfer unit (62) and transfer arm assembly (86) in response to the sensors (91) using the actuators. A communication link is established between the actuators, sensors and controller (101). Preferably, the communication link is a fiber optic link.



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TITLE OF THE INVENTION

SEMICONDUCTOR PROCESSING APPARATUS HAVING LINEAR CONVEYOR SYSTEM

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a continuation-in-part of U.S.S.N. ___ (Corporate Docket No. P96-0018) and of U.S.S.N. ___ (Corporate Docket No. P96-0011) which are hereby incorporated by reference.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not Applicable

BACKGROUND OF THE INVENTION

In the production of semiconductor integrated circuits and other semiconductor articles from semiconductor wafers, it is often necessary to provide multiple metal layers on the wafer to serve as interconnect metallization which electrically connects the various devices on the integrated circuit to one another. Traditionally, aluminum has been used for such interconnects, however, it is now recognized that copper metallization may be preferable.

The application of copper onto semiconductor wafers has, in particular, proven to be a great technical challenge. At this time copper metallization has not achieved commercial reality due to practical problems of forming copper layers on semiconductor devices in a reliable and cost efficient manner. This is caused, in part, by the relative difficulty in performing reactive ion etching or other selective removal of copper at reasonable production temperatures. The

selective removal of copper is desirable to form patterned layers and provide electrically conductive interconnects between adjacent layers of the wafer or other wafer.

Because reactive ion etching cannot be efficiently used, the industry has sought to overcome the problem of forming patterned layers of copper by using a damascene electroplating process where holes, more commonly called vias, trenches and other recesses are used in which the pattern of copper is desired. In the damascene process, the wafer is first provided with a metallic seed layer which is used to conduct electrical current during a subsequent metal electroplating step. The seed layer is a very thin layer of metal which can be applied using one or more of several processes. For example, the seed layer of metal can be laid down using physical vapor deposition or chemical vapor deposition processes to produce a layer on the order of 1000 angstroms thick. The seed layer can advantageously be formed of copper, gold, nickel, palladium, and most or all other metals. The seed layer is formed over a surface which is convoluted by the presence of the vias, trenches, or other device features which are recessed. This convoluted nature of the exposed surface provides increased difficulties in forming the seed layer in a uniform manner. Nonuniformities in the seed layer can result in variations in the electrical current passing from the exposed surface of the wafer during the subsequent electroplating process. This in turn can lead to nonuniformities in the copper layer which is subsequently electroplated onto the seed layer. Such nonuniformities can cause deformities and failures in the resulting semiconductor device being formed.

In damascene processes, the copper layer that is electroplated onto the seed layer is in the form of a blanket layer. The blanket layer is plated to an extent which forms an overlying layer, with the goal of completely providing a copper layer that fills the trenches and vias and extends a certain amount above these features. Such a blanket layer will typically be formed in

thicknesses on the order of 10,000-15,000 angstroms (1-1.5 microns).

The damascene processes also involve the removal of excess metal material present outside of the vias, trenches or other recesses. The metal is removed to provide a resulting patterned metal layer in the semiconductor integrated circuit being formed. The excess plated material can be removed, for example, using chemical mechanical planarization. Chemical mechanical planarization is a processing step which uses the combined action of a chemical removal agent and an abrasive which grind and polish the exposed metal surface to remove undesired parts of the metal layer applied in the electroplating step.

Automation of the copper electroplating process has been elusive, and there is a need in the art for improved semiconductor plating systems which can produce copper layers upon semiconductor articles which are uniform and can be produced in an efficient and cost-effective manner. More particularly, there is a substantial need to provide a copper plating system that is effectively and reliably automated.

BRIEF SUMMARY OF THE INVENTION

A transport system for manipulating a semiconductor wafer in a processing tool is set forth. The system includes a transport unit guide disposed within the processing tool for supporting a wafer transfer unit as the unit moves between a first position and a second position. The transport unit guide comprises a frame, a lateral guide rail mounted on the frame, and a series of magnetic segments arranged upon the transport unit guide proximate the lateral guide rail. The wafer transfer unit includes a tram translatably attached to the lateral guide rail and a wafer transfer arm assembly for manipulating the semiconductor wafer. An electromagnet is mounted on the tram in cooperative relation with the magnetic segments for moving the transfer unit along the guide rail. Actuators are used for controlling the position of the transfer unit and transfer arm assembly, and sensors are used for determining the position of the transfer unit and the transfer arm assembly. A controller is disposed remote of the wafer transfer unit and directs the movement of the transfer unit and transfer arm assembly in response to the sensors using the actuators. A communication link is established between the actuators, sensors and controller. Preferably, the communication link is a fiber optic link.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Fig. 1 is an isometric view of the semiconductor wafer processing tool in accordance with the present invention.

Fig. 2 is a cross-sectional view taken along line 2-2 of the semiconductor wafer processing tool shown in Fig. 1.

Figs. 3-8 are a diagrammatic representation of a wafer cassette turnstile and elevator of a preferred interface module of the semiconductor wafer processing tool according to the present invention operating to exchange wafer cassettes between a hold position and an extraction position.

Fig. 9 is an isometric view of a preferred wafer cassette tray engageable with the turnstile of an interface module of the semiconductor wafer processing tool.

Figs. 10-15 illustrate one manner in which the processing tool may be modularized to facilitate end-to-end connection of sequential processing units.

Figs. 16-19 illustrate a wafer conveying system in accordance with one embodiment of the present invention.

Figs. 20-25 illustrate a further wafer conveying system in accordance with a further embodiment of the present invention.

Fig. 26 is a functional block diagram of an embodiment of a control system of the semiconductor wafer processing tool.

Fig. 27 is a functional block diagram of a master/slave control configuration of an interface module control subsystem for controlling a wafer cassette interface module.

Fig. 28 is a functional block diagram of an interface module control subsystem coupled with components of a wafer cassette interface module of the processing tool.

Fig. 29 is a functional block diagram of a wafer conveyor control subsystem coupled with components of a wafer conveyor of the processing tool.

Fig. 30 is a functional block diagram of a wafer processing module control subsystem coupled with components of a wafer processing module of the processing tool.

Fig. 31 is a functional block diagram of a slave processor of the interface module control subsystem coupled with components of a wafer interface module of the processing tool.

Fig. 32 is a functional block diagram of a slave processor of the wafer conveyor control subsystem coupled with components of a wafer conveyor of the processing tool.

Fig. 33 is a cross-sectional view of a processing station for use in electroplating a downward facing surface of a semiconductor wafer.

DETAILED DESCRIPTION OF THE INVENTION

Referring to Fig. 1, a present preferred embodiment of the semiconductor wafer processing tool 10 is shown. The processing tool 10 may comprise an interface section 12 and processing section 14. Semiconductor wafer cassettes 16 containing a plurality of semiconductor wafers, generally designated W, may be loaded into the processing tool 10 or unloaded therefrom via the interface section 12. In particular, the wafer cassettes 16 are preferably loaded or unloaded through at least one port such as first port 32 within a front outwardly facing wall of the processing tool 10. An additional second port 33 may be provided within the interface section 12 of the processing tool 10 to improve access and port 32 may be utilized as an input and port 33 may be utilized as an output.

Respective powered doors 35, 36 may be utilized to cover access ports 32, 33 thereby isolating the interior of the processing tool 10 from the clean room. Each door 35, 36 may comprise two portions. The upper portions and lower portion move upward and downward, respectively, into the front surface of the processing tool 10 to open ports 32, 33 and permit access therein.

Wafer cassettes 16 are typically utilized to transport a plurality of semiconductor wafers. The wafer cassettes 16 are preferably oriented to provide the semiconductor wafers therein in an upright or vertical position for stability during transportation of the semiconductor wafers into or out of the processing tool 10.

The front outwardly facing surface of the processing tool 10 may advantageously join a clean room to minimize the number of harmful contaminants which may be introduced into the processing tool 10 during insertion and removal of wafer cassettes 16. In addition, a

plurality of wafer cassettes 16 may be introduced into processing tool 10 or removed therefrom at one time to minimize the opening of ports 32, 33 and exposure of the processing tool 10 to the clean room environment.

The interface section 12 joins a processing section 14 of the processing tool 10. The processing section 14 may include a plurality of semiconductor wafer processing modules for performing various semiconductor process steps. In particular, the embodiment of the processing tool 10 shown in Fig. 1 includes a plating module 20 defining a first lateral surface of the processing section 14. The processing section 14 of the tool 10 may advantageously include additional modules, such as pre-wet module 22 and resist strip module 24, opposite the plating module 20.

Alternatively, other modules for performing additional processing functions may also be provided within the processing tool 10. The specific processing performed by processing modules of the processing tool 10 may be different or of similar nature. Various liquid and gaseous processing steps can be used in various sequences. The processing tool 10 is particularly advantageous in allowing a series of complex processes to be run serially in different processing modules set up for different processing solutions. All the processing can be advantageously accomplished without human handling and in a highly controlled working space 11, thus reducing human operator handling time and the chance of contaminating the semiconductor wafers.

The processing modules of the process tool 10 are preferably modular, interchangeable, stand-alone units. The processing functions performed by the processing tool 10 may be changed after installation of the processing tool 10 increasing flexibility and

allowing for changes in processing methods. Additional wafer processing modules may be added to the processing tool 10 or replace existing processing modules 19.

The processing tool 10 of the present invention preferably includes a rear closure surface 18 joined with the lateral sides of the processing tool 10. As shown in Fig. 1, an air supply 26 may be advantageously provided intermediate opposing processing modules of the processing section 14. The interface section 12, lateral sides of the processing section 14, closure surface 18, and air supply 26 preferably provide an enclosed work space 11 within the processing tool 10. The air supply 26 may comprise a duct coupled with a filtered air source (not shown) for providing clean air into the processing tool 10. More specifically, the air supply 26 may include a plurality of vents intermediate the processing modules 19 for introducing clean air into work space 11.

Referring to Fig. 16, exhaust ducts 58, 59 may be provided adjacent the frame 65 of a wafer transport unit guide 66 to remove the circulated clean air and the contaminants therein. Exhaust ducts 58, 59 may be coupled with the each of the processing modules 19 for drawing supplied clean air therethrough. In particular, clean air is supplied to the workspace 11 of the processing tool 10 via air supply 26. The air may be drawn adjacent the wafer transport units 62, 64 and into the processing modules 19 via a plurality of vents 57 formed within a shelf or process deck thereof by an exhaust fan (not shown) coupled with the output of exhaust ducts 58, 59. Each processing module 19 within the processing tool 10 may be directly coupled with ducts 58, 59. The air may be drawn out of the ducts 58, 59 of the processing tool 10 through the rear closant surface 18 or through a bottom of surface of the processing tool 10. Providing an enclosed work space and controlling the environment within the work space

greatly reduces the presence of contaminants in the processing tool 10.

Each of the processing modules may be advantageously accessed through exterior panels of the respective modules forming the lateral side of the processing tool 10. The lateral sides of the processing tool 10 may be adjacent a gray room environment. Gray rooms have fewer precautions against contamination compared with the clean rooms. Utilizing this configuration reduces plant costs while allowing access to the processing components and electronics of each wafer module of the processing tool 10 which require routine maintenance.

A user interface 30 may be provided at the outwardly facing front surface of the processing tool as shown in Fig. 1. The user interface 30 may advantageously be a touch screen cathode ray tube control display allowing finger contact to the display screen to effect various control functions within the processing tool 10. An additional user interface 30 may also be provided at the rear of the processing tool 10 or within individual processing modules so that processing tool 10 operation can be effected from alternate locations about the processing tool 10. Further, a portable user interface 30 may be provided to permit an operator to move about the processing tool 10 and view the operation of the processing components therein. The user interface 30 may be utilized to teach specified functions and operations to the processing modules 19 and semiconductor wafer transport units 62, 64.

Each module 20, 22, 24 within the processing tool 10 preferably includes a window 34 allowing visual inspection of processing tool 10 operation from the gray room. Further, vents 37 may be advantageously provided within a top surface of each processing module 20, 22, 24. Processing module electronics are preferably located adjacent the vents 37 allowing

circulating air to dissipate heat generated by such electronics.

The work space 11 within the interface section 12 and processing section 14 of an embodiment of the processing tool 10 is shown in detail in Fig. 2.

The interface section 12 includes two interface modules 38, 39 for manipulating wafer cassettes 16 within the processing tool 10. The interface modules 38, 39 receive wafer cassettes 16 through the access ports 32, 33 and may store the wafer cassettes 16 for subsequent processing of the semiconductor wafers therein. In addition, the interface modules 38, 39 store the wafer cassettes for removal from the processing tool 10 upon completion of the processing of the semiconductor wafers within the respective wafer cassette 16.

Each interface module 38, 39 may comprise a wafer cassette turnstile 40, 41 and a wafer cassette elevator 42, 43. The wafer cassette turnstiles 40, 41 generally transpose the wafer cassettes 16 from a stable vertical orientation to a horizontal orientation where access to the semiconductor wafers is improved. Each wafer cassette elevator 42, 43 has a respective wafer cassette support 47, 48 for holding wafer cassettes 16. Each wafer cassette elevator 42, 43 is utilized to position a wafer cassette 16 resting thereon in either a transfer position and extraction position. The operation of the wafer interface modules 38, 39 is described in detail below.

In a preferred embodiment of the present invention, the first wafer interface module 38 may function as an input wafer cassette interface for receiving unprocessed semiconductor wafers into the processing tool 10. The second wafer interface module 39 may function as an output wafer cassette interface for holding processed semiconductor wafers for removal from the processing tool 10. Wafer transport units 62, 64 within the processing tool 10 may access

wafer cassettes 16 held by either wafer interface module 38, 39. Such an arrangement facilitates transferring of semiconductor wafers throughout the processing tool 10.

A semiconductor wafer conveyor 60 is shown intermediate processing modules 20, 22, 24 and interface modules 38, 39 in Fig. 2. The wafer conveyor 60 includes wafer transport units 62, 64 for transferring individual semiconductor wafers W between each of the wafer interface modules 38, 39 and the wafer processing modules 19.

Wafer conveyor 60 advantageously includes a transport unit guide 66, such as an elongated rail, which defines a plurality of paths 68, 70 for the wafer transport units 62, 64 within the processing tool 10. A wafer transport unit 62 on a first path 68 may pass a wafer transport unit 64 positioned on a second path 70 during movement of the transport units 62, 64 along transport guide 66. The processing tool 10 may include additional wafer transport units to facilitate the transfer of semiconductor wafers W between the wafer processing modules 20, 22, 24 and wafer interface modules 38, 39.

More specifically, the second arm extension 88 may support a semiconductor wafer W via vacuum support 89. The appropriate wafer transport unit 62, 64 may approach a wafer support 401 by moving along transport unit guide 66. After reaching a proper location along guide 66, the first extension 87 and second extension 88 may rotate to approach the wafer support 401. The second extension 88 is positioned above the wafer support 401 and subsequently lowered toward engagement finger assemblies 409 on the wafer support 401. The vacuum is removed from vacuum support 89, and finger assemblies within the processing modules grasp the semiconductor wafer W positioned therein. Second extension 88 may be lowered and removed from beneath the semiconductor wafer held by the wafer engagement

fingers.

Following completion of processing of the semiconductor wafer within the appropriate processing module 20, 22, 24, a wafer transport unit 62, 64 may retrieve the wafer and either deliver the wafer to another processing module 20, 22, 24 or return the wafer to a wafer cassette 16 for storage or removal from the processing tool 10.

Each of the wafer transport units 62, 64 may access a wafer cassette 16 adjacent the conveyor 60 for retrieving a semiconductor wafer from the wafer cassette 16 or depositing a semiconductor wafer therein. In particular, wafer transport unit 62 is shown withdrawing a semiconductor wafer W from wafer cassette 16 upon elevator 42 in Fig. 2. More specifically, the second extension 88 and vacuum support 89 connected therewith may be inserted into a wafer cassette 16 positioned in the extraction position. Second extension 88 and vacuum support 89 enter below the lower surface of the bottom semiconductor wafer W held by wafer cassette 16. A vacuum may be applied via vacuum support 89 once support 89 is positioned below the center of the semiconductor wafer W being removed. The second extension 88, vacuum support 89 and semiconductor wafer W attached thereto may be slightly raised via transfer arm elevator 90. Finally, first extension 87 and second extension 88 may be rotated to remove the semiconductor wafer W from the wafer cassette 16. The wafer transport unit 62, 64 may thereafter deliver the semiconductor wafer W to a wafer processing module 19 for processing.

Thereafter, wafer transport unit 62 may travel along path 68 to a position adjacent an appropriate processing module 20, 22, 24 for depositing the semiconductor wafer upon wafer processing support 401 for processing of the semiconductor wafer.

INTERFACE MODULE

Referring to Fig. 3 - Fig. 8, the operation of the interface module 38 is shown in detail. The following discussion is limited to wafer interface module 38 but is also applicable to wafer interface module 39 inasmuch as each interface module 38, 39 may operate in substantially the same manner.

Preferably, the first wafer interface module 38 and the second wafer interface module 39 may function as a respective semiconductor wafer cassette 16 input module and output module of the processing tool 10. Alternately, both modules can function as both input and output. More specifically, wafer cassettes 16 holding unprocessed semiconductors wafers may be brought into the processing tool 10 via port 32 and temporarily stored within the first wafer interface module 38 until the semiconductor wafers are to be removed from the wafer cassette 16 for processing. Processed semiconductor wafers may be delivered to a wafer cassette 16 within the second wafer interface module 39 via wafer transport units 62, 64 for temporary storage and/or removal from the processing tool 10.

The wafer interface modules 38, 39 may be directly accessed by each of the wafer transport units 62, 64 within the processing tool 10 for transferring semiconductor wafers therebetween. Providing a plurality of wafer cassette interface modules 38, 39 accessible by each wafer transport unit 62, 64 facilitates the transport of semiconductor wafers W throughout the processing tool 10 according to the present invention.

Each wafer interface module 38, 39 preferably includes a wafer cassette turnstile 40 and a wafer cassette elevator 42 adjacent thereto. The access ports 32, 33 are adjacent the

respective wafer cassette turnstiles 40, 41. Wafer cassettes 16 may be brought into the processing tool 10 or removed therefrom via ports 32, 33.

Wafer cassettes 16 are preferably placed in a vertical position onto cassette trays 50 prior to delivery into the processing tool 10. Cassette trays 50 are shown in detail in Fig. 9. The vertical position of wafer cassettes 16 and the semiconductor wafers therein provides a secure orientation to maintain the semiconductor wafers within the wafer cassette 16 for transportation.

Each wafer cassette turnstile 40, 41 preferably includes two saddles 45, 46 each configured to hold a wafer cassette 16. Providing two saddles 45, 46 enables two wafer cassettes 16 to be placed into the processing tool 10 or removed therefrom during a single opening of a respective access door 35, 36 thereby minimizing exposure of the workspace 11 within the processing tool 10 to the clean room environment.

Each saddle 45, 46 includes two forks engageable with the cassette tray 50. Saddles 45, 46 are powered by motors within the wafer cassette turnstile shaft 49 to position the wafer cassette 16 in a horizontal or vertical orientation. The wafer cassettes 16 and semiconductor wafers therein are preferably vertically oriented for passage through the access ports 32, 33 and horizontally oriented in a transfer or extraction position to provide access of the wafers therein to the wafer transport units 62, 64.

The wafer cassette 16 held by wafer cassette turnstile 40 in Fig. 3, also referred to as wafer cassette 15, is in a hold position (also referred to herein as a load position). The semiconductor wafers within a wafer cassette 16 in the hold position may be stored for subsequent processing. Alternatively, the semiconductor wafers within a wafer cassette 16 in

the hold position may be stored for subsequent removal from the processing tool 10 through an access port 32, 33.

Referring to Fig. 3, the wafer cassette 16 supported by the wafer cassette elevator 42, also referred to as wafer cassette 17, is in an extraction or exchange position. Semiconductor wafers may either be removed from or placed into a wafer cassette 16 positioned in the extraction position via a wafer transport unit 62, 64.

The wafer cassette turnstile 41 and wafer cassette elevator 42 may exchange wafer cassettes 15, 17 to transfer a wafer cassette 17 having processed semiconductor wafers therein from the extraction position to the hold position for removal from the processing tool 10. Additionally, such an exchange may transfer a wafer cassette 15 having unprocessed semiconductor wafers therein from the hold position to the extraction position providing wafer transport units 62, 64 with access to the semiconductor wafer therein.

The exchange of wafer cassettes 15, 17 is described with reference to Fig. 4 - Fig. 8. Specifically, saddle 46 is positioned below a powered shaft 44 of wafer cassette elevator 42. Shaft 44 is coupled with a powered wafer cassette support 47 for holding a wafer cassette 16. Shaft 44 and wafer cassette support 47 attached thereto are lowered as shown in Fig. 4 and shaft 44 passes between the forks of saddle 46.

Referring to Fig. 5, a motor within shaft 44 rotates wafer cassette support 47 about an axis through shaft 44 providing the wafer cassette 17 thereon in an opposing relation to the wafer cassette 15 held by wafer cassette turnstile 40. Both saddles 45, 46 of wafer cassette turnstile 40 are subsequently tilted into a horizontal orientation as shown in Fig. 6. The shaft 44 of wafer cassette elevator 42 is next lowered and wafer cassette 17 is brought into

engagement with saddle 46 as depicted in Fig. 7. The shaft 44 and wafer cassette support 47 are lowered an additional amount to clear rotation of wafer cassettes 16. Referring to Fig. 8, wafer cassette turnstile 40 rotates 180 degrees to transpose wafer cassettes 15, 17.

Wafer cassette 17 having processed semiconductor wafers therein is now accessible via port 32 for removal from the processing tool 10. Wafer cassette 15 having unprocessed semiconductors therein is now positioned for engagement with wafer cassette support 47. The transfer process steps shown in Fig. 3 - Fig. 8 may be reversed to elevate the wafer cassette 15 into the extraction position providing access of the semiconductor wafers to wafer transport units 62, 64.

Figure 10 illustrates one manner in which the apparatus 10 may be modularized. As illustrated, the apparatus 10 is comprised of an input/output assembly 800, left and right processing modules 805, 810, wafer conveyor system 60, top exhaust assembly 820, and end panel 825. As illustrated, left and right processing modules 805 and 810 may be secured to one another about the wafer conveying system 60 to form a processing chamber having an inlet and 830 and an outlet 835. A plurality of these processing modules may thus be secured in an end-to-end configuration to thereby provide an extended processing chamber capable of performing a substantially larger number of processes on each wafer or, in the alternative, process a larger number of wafers concurrently. In such instances, the wafer conveying system 60 of one apparatus 10 is programmed to cooperate with the wafer conveying system 60 of one or more prior or subsequent conveying systems 60.

Figure 11 illustrates one manner of arranging processing heads within the apparatus 10. In this embodiment, the left hand processing module 805 is comprised of three

processing heads that are dedicated to rinsing and drying each wafer after electrochemical deposition and two processing heads for performing wetting of the wafers prior to electrochemical deposition. Generically, the left hand processing module 805 constitutes a support module having processing heads used in pre-processing and post-processing of the wafers with respect to electrochemical copper deposition. The right-hand module 810 generically constitutes a plating module and includes five reactor heads dedicated to electrochemical copper deposition. In the embodiment of Figure 11, a wafer alignment station 850 is provided to ensure thickness proper orientation of each wafer as it is processed in the apparatus. Wafer alignment may be based upon sensing of registration marks or the like on each wafer.

Figures 12 and 13 illustrate embodiments of the left and right hand processing modules 805 and 810, respectively. In these figures, the exterior portions of the respective housing have been removed thereby exposing various system components. Preferably, electronic components such as power supplies, controllers, etc., are disposed in the upper portion of each of the processing modules 805 and 810, while moving components and the like are disposed in a lower portion of each of the processing modules.

Figure 14 is a perspective view of the input module 800 with its panels removed as viewed from the interior of apparatus 10. Figure 15 provides a similar view of the input module 800 with respect to the exterior of apparatus 10. In the illustrated embodiment, the wafer alignment station 850 and a wafer alignment controller 860 are provided in the input module 800. A robot controller 865 used to control the wafer conveying system 60 is also disposed therein. To keep track of the wafers as they are processed, the input module 800

is provided with one or more wafer mapping sensors 870 that sense the wafers present in each cassette. Other components in the input module 800 include the system control computer 875 and a four-axis controller 880. The system control computer 875 is generally responsible for coordinating all operations of the apparatus 10.

SEMICONDUCTOR WAFER CONVEYOR

The processing tool 10 includes a semiconductor wafer conveyor 60 for transporting semiconductor wafers throughout the processing tool 10. Preferably, semiconductor wafer conveyor 60 may access each wafer cassette interface module 38, 39 and each wafer processing module 19 within processing tool 10 for transferring semiconductor wafers therebetween. This includes processing modules from either side.

One embodiment of the wafer conveyor system 60 is depicted in Fig. 16. The wafer conveyor 60 generally includes a wafer transport unit guide 66 which preferably comprises an elongated spine or rail mounted to frame 65. Alternatively, transport unit guide 66 may be formed as a track or any other configuration for guiding the wafer transport units 62, 64 thereon. The length of wafer conveyor 60 may be varied and is configured to permit access of the wafer transport units 62, 64 to each interface module 38, 39 and processing modules 20, 22, 24.

Wafer transport unit guide 66 defines the paths of movement 68, 70 of wafer transport units 62, 64 coupled therewith. Referring to Fig. 16, a spine of transport unit guide 66 includes guide rails 63, 64 mounted on opposite sides thereof. Each semiconductor wafer transport unit 62, 64 preferably engages a respective guide rail 63, 64. Each guide rail can

mount one or more transport units 62, 64. Extensions 69, 75 may be fixed to opposing sides of guide 66 for providing stability of the transport units 62, 64 thereagainst and to protect guide 66 from wear. Each wafer transport unit 62, 64 includes a roller 77 configured to ride along a respective extension 69, 75 of guide 66.

It is to be understood that wafer conveyor 60 may be formed in alternate configurations dependent upon the arrangement of interface modules 38, 39 and processing modules 20, 22, 24 within the processing tool 10. Ducts 58, 59 are preferably in fluid communication with extensions from each wafer processing module 19 and an exhaust fan for removing circulated air from the workspace 11 of the processing tool 10.

Each wafer transport unit 62, 64 is powered along the respective path 68, 70 by a suitable driver. More specifically, drive operators 71, 74 are mounted to respective sides of transport unit guide 66 to provide controllable axial movement of wafer transport units 62, 64 along the transport unit guide 66.

The drive operators 71, 74 may be linear magnetic motors for providing precise positioning of wafer transport units 62, 64 along guide 66. In particular, drive operators 71, 74 are preferably linear brushless direct current motors. Such preferred driver operators 71, 74 utilize a series of angled magnetic segments which magnetically interact with a respective electromagnet 79 mounted on the wafer transport units 62, 64 to propel the units along the transport unit guide 66.

Cable guards 72, 73 may be connected to respective wafer transport units 62, 64 and frame 65 for protecting communication and power cables therein. Cable guards 72, 73 may comprise a plurality of interconnected segments to permit a full range of motion of wafer

transport units 62, 64 along transport unit guide 66.

As shown in Fig. 17, a first wafer transport unit 62 is coupled with a first side of the spine of guide 66. Each wafer transport unit 62, 64 includes a linear bearing 76 for engagement with linear guide rails 63, 64. Further, the wafer transport units 62, 64 each preferably include a horizontal roller 77 for engaging a extension 69 formed upon the spine of the guide 66 and providing stability.

Fig. 17 additionally shows an electromagnet 79 of the first wafer transport unit 62 mounted in a position to magnetically interact with drive actuator 71. Drive actuator 71 and electromagnet 79 provide axial movement and directional control of the wafer transport units 62, 64 along the transport unit guide 66.

SEMICONDUCTOR WAFER TRANSPORT UNITS

Preferred embodiments of the semiconductor wafer transport units 62, 64 of the wafer conveyor 60 are described with reference to Fig. 18 and Fig. 19.

In general, each wafer transport unit 62, 64 includes a movable carriage or tram 84 coupled to a respective side of the transport unit guide 66, a wafer transfer arm assembly 86 movably connected to the tram 84 for supporting a semiconductor wafer W, and a wafer transfer arm elevator 90 for adjusting the elevation of the transfer arm assembly 86 relative to tram 84.

Referring to Fig. 18, a cover 85 surrounds the portion of tram 84 facing away from the transport unit guide 66. Tram 84 includes linear bearings 76 for engagement with respective guide rails 63, 64 mounted to transport unit guide 66. Linear bearings 76 maintain

the tram 84 in a fixed relation with the transport unit guide 66 and permit axial movement of the tram 84 therealong. A roller 77 engages a respective extension 69 for preventing rotation of tram 84 about guide rail 63, 64 and providing stability of wafer transport unit 62. The electromagnet 79 is also shown connected with the tram 84 in such a position to magnetically interact with a respective transport unit 62, 64 drive actuator 71, 74.

A wafer transfer arm assembly 86 extends above the top of tram 84. The wafer transfer arm assembly 86 may include a first arm extension 87 coupled at a first end thereof with a shaft 83. A second arm extension 88 may be advantageously coupled with a second end of the first extension 87. The first arm extension 87 may rotate 360 degrees about shaft 83 and second arm extension 88 may rotate 360 degrees about axis 82 passing through a shaft connecting first and second arm extensions 87, 88.

Second extension 88 preferably includes a wafer support 89 at a distal end thereof for supporting a semiconductor wafer W during the transporting thereof along wafer conveyor 60. The transfer arm assembly 86 preferably includes a chamber coupled with the wafer support 89 for applying a vacuum thereto and holding a semiconductor wafer W thereon.

Providing adjustable elevation of transfer arm assembly 86, rotation of first arm extension 87 about the axis of shaft 83, and rotation of second extension 88 about axis 82 allows the transfer arm 86 to access each semiconductor wafer holder 810 of all processing modules 19 and each of the wafer cassettes 16 held by interface modules 38, 39 within the processing tool 10. Such access permits the semiconductor wafer transport units 62, 64 to transfer semiconductor wafers therebetween.

The cover 85 has been removed from the wafer transport unit shown in Fig. 19 to

reveal a wafer transfer arm elevator 90 coupled with tram 84 and transfer arm assembly 86. Transfer arm elevator 90 adjusts the vertical position of the transfer arm assembly 86 relative to the tram 84 during the steps of transferring a semiconductor wafer between the wafer support 89 and one of a wafer holder 810 and the wafer cassette 16.

The path position of the tram 84 of each wafer transport unit 62, 64 along the transport unit guide 66 is precisely controlled using a positional indicating array, such as a CCD array 91 of Fig. 19. In one embodiment of the processing tool 10, each semiconductor wafer holder 810 within a processing module 19 has a corresponding light or other beam emitter 81 mounted on a surface of the processing module 19 as shown in Fig. 2 for directing a beam of light toward the transport unit guide 66. The light emitter 81 may present a continuous beam or alternatively may be configured to generate the beam as a wafer transport unit 62, 64 approaches the respective wafer holder 810.

The transfer arm assembly 86 includes an CCD array 91 positioned to receive the laser beam generated by light emitter 81. A position indicating array 91 on shaft 83 detects the presence of the light beam to determine the location of tram 84 along transport unit guide 66. The positional accuracy of the wafer transport unit position indicator is preferably in the range less than 0.003 inch (approximately less than 0.1 millimeter).

A second embodiment of a wafer transport unit 562b is shown in Figs. 20-25 and is similarly provided with a movable carriage or tram 584 coupled to a respective side of the transport unit guide 66, a wafer transfer arm assembly 586 movably connected to the tram 584 for supporting a semiconductor wafer W, and a wafer transfer arm elevator 590 for adjusting the elevation of the transfer arm assembly 586 relative to tram 584. A cover 585 surrounds a

portion of tram 584. Tram 584 includes linear bearings 576 for engagement with respective guide rails 63, 64 mounted to transport unit guide 66. Linear bearings 576 maintain the tram 584 in a fixed relation with the transport unit guide 66 and permit axial movement of the tram 584 therealong. The electromagnet 579 magnetically interacts with the guide 66 to drive actuator 71, 74.

A wafer transfer arm assembly 586 extends above the top of tram 584. The wafer transfer arm assembly 586 includes a first arm extension 587 coupled at a first end thereof with a shaft 583. A second arm extension 588, having a wafer support 589 for supporting the semiconductor wafer W, may be advantageously coupled with a second end of the first extension 587. The first arm extension 587 may rotate 360 degrees about shaft 583 and second arm extension 588 may rotate 360 degrees about axis 582 passing through a shaft connecting first and second arm extensions 587, 588.

As with the first embodiment, providing adjustable elevation of transfer arm assembly 586, rotation of first arm extension 587 about the axis of shaft 583, and rotation of second extension 588 about axis 582 permits the semiconductor wafer transport units 562a, 562b to transfer semiconductor wafers therebetween.

As shown in Fig. 21, cover 585 has been removed from the wafer transport unit 562b, revealing a wafer transfer arm elevator 590 coupled with tram 584 and transfer arm assembly 586. Transfer arm elevator 590 adjusts the vertical position of the transfer arm assembly 586 relative to the tram 584 during a transfer of a semiconductor wafer.

In the second embodiment of the wafer transport units 562a, 562b, a fiber optic communication path, such as a fiber optic filament, replaces wires 72, 73 to the wafer

transport units through a digital-to-analog converter board 540 on each of the wafer transport units 562a, 562b. The use of fiber optics as opposed to wire harnesses lowers the inertial mass of the transport units 562a, 562b and improves reliability. Preferably, such communications take place between the transfer unit and the system controller 875.

The path and operational position of the tram 584 of each wafer transport unit 562a, 562b along the transport unit guide 66 is precisely controlled using a combination of encoders to provide position information on the position of the tram 584, transfer arm assembly 586 and second extension 588 in three-axis space. An absolute encoder, the position of which is shown at 591, is located in the elevator 590. An absolute encoder, TPOW, is shown at 592, located in the base motor 593 of the shaft 583. An absolute encoder, TPOW, is shown at 594, located in the shaft 583. Wrist absolute encoder, the position of which is shown at 595, is located at the distal end of transfer arm assembly 586. An elbow absolute encoder, TPOWISA, 597 is provided at the base of the shaft 583. Lift absolute encoder 596 is located along the base motor 593. A linear encoder 598, head rail encoder 599 and track CDD array absolute encoder 541 are located on the base plate 203 of the base of tram 584, the latter located for sensing the beam emitter 81 mounted on a surface of the processing module 19 as shown in Fig. 2 and discussed above. The foregoing allows precise and reliable positional accuracy.

Mounting of the wafer transport units is shown in Figure 22. As illustrated, a wafer conveyor 560 includes a wafer transport unit guide 566 which comprises an elongated spine or rail mounted to frame 565. Wafer transport unit guide 566 defines the paths of movement 568, 570 of wafer transport units 544a, 544b. A spine of transport unit guide 566 includes

upper guide rails 563a, 564a and lower guide rails 563b, 564b mounted on opposite sides thereof. Each semiconductor wafer transport unit 544a, 544b preferably engages each of the respective upper guide rails 563a, 564b and lower guide rails 563b, 564b. Each of the pair of upper and lower guide rails can mount one or more transport units 544a, 544b.

Each wafer transport unit 544a, 544b is also powered along the respective path 568, 570 by drive operators 571, 574 mounted to respective sides of transport unit guide 66 to provide controllable axial movement of wafer transport units 544a, 544b along the transport unit guide 566. The drive operators 571, 574 may be linear magnetic motors for providing precise positioning of wafer transport units 544a, 544b along guide 566, and are again preferably linear brushless direct current motors utilizing a series of angled magnetic segments which magnetically interact with a respective electromagnet 579 mounted on each of the wafer transport units 544a, 544b to propel the units along the transport unit guide 566.

Fiber optic cable guards 572, 573 provide communication with the respective wafer transport units 544a, 544b and protect fiber optic cables located therein. Cable guards 572, 573 may comprise a plurality of interconnected segments to permit a full range of motion of wafer transport units 544a, 544b along transport unit guide 566.

As shown in Fig. 22, wafer transport units 544a, 544b are coupled along each side of the spine of guide 566. Each wafer transport unit 544a, 544b includes an upper linear bearing 576a for engagement with upper linear guide rails 563a, 564a, respectively. Further, each wafer transport units 544a, 544b includes a lower linear bearing 576b engaging the lower linear guide rails 563b, 564b, providing stability and more equal distribution of the weight loads upon the rails.

With reference to Figs. 22-24, the upper and lower linear bearing 576a, 576b also provides a means by which the vertical axis of the wafer transfer arm assembly 586 extending above the top of tram 584 may be adjusted. It is important that the transfer arm assembly 586 rotate in a plane as close as possible to the absolute horizontal plane during the transfer of wafers within the processing tool 10. To this end, the lower elbow housing 210 of the transfer arm assembly, shown in Fig. 25, mounted to the base plate 203 of the transport unit 544a is provided with a tilt adjustment.

The lower elbow housing 210 is mounted to a base plate 211, as seen in Figs. 21, 23 and 24 through upper mounting screws 212 and lower mounting screws 214. The base plate 211 is in turn fastened to the elevator motor 590 to raise or lower the transfer arm assembly 586, better seen in Fig. 25. As seen in Fig. 26, positioned laterally between the upper mounting screws 212 are embossed pivots 216 on the base plate 211 that engage a corresponding, yet slightly smaller, lateral groove 218 on the lower elbow housing 210. The pivots 216 are preferably sized, relative the lateral groove 218 to provide a clearance between the base plate 211 and the lower elbow housing 210 so that about 0.95 degrees of tilt is available between the two. In combination with one or more leveling screws 220 and the upper and lower mounting screws 212, 214, the angular orientation of the lower elbow housing 210, and the attached transfer arm assembly 586, can be adjusted and fixed to provide rotation of the transfer arm assembly 586 as close as possible within the absolute horizontal plane during the transfer of wafers within the processing tool 10.

Also, compliant attachment of the lower linear bearing guides 576b is important to smooth operation of the wafer transport unit 544a, 544b along the guide 566. Providing such

compliant attachment, preferably allowing 0.100 inch of float, at the lower gearing guides 576b is obtained by use of a compliant fastening technique. A float pin 221 is positioned about mounting screw 222, with an O-ring 223, preferably VITON, positioned about the float pin. When installed within shouldered counterbore 224 of the base plate 203 into tapped hole 227 of lower bearing guide 576b, as shown in Fig. 28, the screw 222 bears against a flange 225 of the float pin 221, which in turn bears against the O-ring 223. The O-ring 223 then bears against the shoulder 226 of the counterbore. However, even when the screw 222 is tightened, relative motion is allowed between the lower bearing guide 576b and the base plate 203 to facilitate smooth motion over the entire guide 566.

CONTROL SYSTEM

Referring to Fig. 26, there is shown one embodiment of the control system 100 of the semiconductor wafer processing tool 10. As illustrated, the control system 100 generally includes at least one grand master controller 101 for controlling and/or monitoring the overall function of the processing tool 10.

The control system 100 is preferably arranged in a hierarchial configuration. The grand master controller 101 includes a processor electrically coupled with a plurality of subsystem control units as shown in Fig. 26. The control subsystems preferably control and monitor the operation of components of the corresponding apparatus (i.e., wafer conveyor 60, processing modules 20, 22, 24, interface modules 38, 39, etc.). The control subsystems are preferably configured to receive instructional commands or operation instructions such as software code from a respective grand master control 101, 102. The control subsystems 110, 113 - 119 preferably provide process and status information to respective grand master

controllers 101, 102.

More specifically, the grand master control 101 is coupled with an interface module control 110 which may control each of the semiconductor wafer interface modules 38, 39. Further, grand master control 101 is coupled with a conveyor control 113 for controlling operations of the wafer conveyor 60 and a plurality of processing module controls 114, 115 corresponding to semiconductor wafer processing modules 20, 22 within the processing tool 10. The control system 100 of the processing tool 10 according to the present disclosure may include additional grand master controllers 102 as shown in Fig. 26 for monitoring or operating additional subsystems, such as additional wafer processing modules via additional processing module control 119. Four control subsystems may be preferably coupled with each grand master controller 101, 102. The grand master controllers 101, 102 are preferably coupled together and each may transfer process data to the other.

Each grand master controller 101, 102 receives and transmits data to the respective modular control subsystems 110 - 119. In a preferred embodiment of the control system 100, a bidirectional memory mapped device is provided intermediate the grand master controller and each modular subsystem connected thereto. In particular, memory mapped devices 160, 161, 162 are provided intermediate the grand master controller 101 and master controllers 130, 131, 132 within respective interface module control 110, wafer conveyor control 113 and processing module control 114.

Each memory mapped device 150, 160 - 162 within the control system 100 is preferably a dual port RAM provided by Cypress for a synchronously storing data. In particular, grand master controller 101 may write data to a memory location corresponding to

master controller 130 and master controller 130 may simultaneously read the data. Alternatively, grand master controller 101 may read data from mapped memory device being written by the master controller 130. Utilizing memory mapped devices 160 - 161 provides data transfer at processor speeds. Memory mapped device 150 is preferably provided intermediate user interface 30 and the grand master controllers 101, 102 for transferring data therebetween.

A user interface 30 is preferably coupled with each of the grand master controllers 101, 102. The user interface 30 may be advantageously mounted on the exterior of the processing tool 10 or at a remote location to provide an operator with processing and status information of the processing tool 10. Additionally, an operator may input control sequences and processing directives for the processing tool 10 via user interface 30. The user interface 30 is preferably supported by a general purpose computer within the processing tool 10. The general purpose computer preferably includes a 486 100 MHz processor, but other processors may be utilized.

Each modular control subsystem, including interface module control 110, wafer conveyor control 113 and each processing module control 114 - 119, is preferably configured in a master/slave arrangement. The modular control subsystems 110, 113 - 119 are preferably housed within the respective module such as wafer interface module 38, 39, wafer conveyor 60, or each of the processing modules 20, 22, 24. The grand master controller 101 and corresponding master controllers 130, 131, 132 coupled therewith are preferably embodied on a printed circuit board or ISA board mounted within the general purpose computer supporting user interface 30. Each grand master controller 101, 102 preferably includes a 68EC000 processor provided by Motorola and each master controller 130 and slave controller within control system 100 preferably includes a 80251 processor provided by Intel.

Each master controller 130, 131, 132 is coupled with its respective slave controllers via a data link 126, 127, 129 as shown in Fig. 27 - Fig. 30. Each data link 126, 127, 129 preferably comprises an optical data medium such as Optilink provided by Hewlett Packard. However, data links 126, 127, 129 may comprise alternate data transfer media.

Referring to Fig. 27, the master/slave control subsystem for the interface module control 110 is illustrated. Each master and related slave configuration preferably corresponds to a single module (i.e., interface, conveyor, processing) within the processing tool 10. However, one master may control or monitor a plurality of modules. The master/slave configuration depicted in Fig. 27 and corresponding to the interface module control 110 may additionally apply to the other modular control subsystems 113, 114, 115.

The grand master controller 101 is connected via memory mapped device 160 to a master controller 130 within the corresponding interface module control 110. The master

controller 130 is coupled with a plurality of slave controllers 140, 141, 142. Sixteen slave controllers may be preferably coupled with a single master controller 130 - 132 and each slave controller may be configured to control and monitor a single motor or process component, or a plurality of motors and process components.

The control system 100 of the processing tool 10 preferably utilizes flash memory. More specifically, the operation instructions or program code for operating each master controller 130 - 132 and slave controller 140 - 147 within the control system 100 may be advantageously stored within the memory of the corresponding grand master controller 101, 102. Upon powering up, the grand master controller 101, 102 may poll the corresponding master controllers 130 -132 and download the appropriate operation instruction program to operate each master controller 130 - 132. Similarly, each master controller 130 - 132 may poll respective slave controllers 140 - 147 for identification. Thereafter, the master controller 130 - 132 may initiate downloading of the appropriate program from the grand master controller 101, 102 to the respective slave controller 140 - 147 via the master controller 130 - 132.

Each slave controller may be configured to control and monitor a single motor or a plurality of motors within a corresponding processing module 19, interface module 38, 39 and wafer conveyor 60. In addition, each slave controller 140 - 147 may be configured to monitor and control process components 184 within a respective module 19. Any one slave controller, such as slave controller 145 shown in Fig. 36, may be configured to control and/or monitor servo motors and process components 184.

Each slave controller includes a slave processor which is coupled with a plurality of

port interfaces. Each port interface may be utilized for control and/or monitoring of servo motors and process components 184. For example, a port may be coupled with a servo controller card 176 which is configured to operate a wafer transfer unit 62a, 62b. The slave processor 171 may operate the wafer transfer unit 62a, 62b via the port and servo controller 176. More specifically, the slave processor 171 may operate servo motors within the wafer transfer unit 62a, 62b and monitor the state of the motor through the servo controller 176.

Alternatively, different slave controllers 140, 141 may operate different components within a single processing tool device, such as interface module 38. More specifically, the interface module control 110 and components of the interface module 38 are depicted in Fig. 32. Slave controller 140 may operate turnstile motor 185 and monitor the position of the turnstile 40 via incremental turnstile encoder 190. Slave controller 140 is preferably coupled with the turnstile motor 185 and turnstile encoder 190 via a servo control card (shown in Fig. 35). Slave controller 141 may operate and monitor saddle 45 of the turnstile 40 by controlling saddle motor 186 and monitoring saddle encoder 191 via a servo control card.

A port of a slave processor may be coupled with an interface controller card 180 for controlling and monitoring process components within a respective processing module 19. For example, a flow sensor 657 may provide flow information of the delivery of processing fluid to a processing bowl within the module. The interface controller 180 is configured to translate the data provided by the flow sensors 657 or other process components into a form which may be analyzed by the corresponding slave processor 172. Further, the interface controller 180 may operate a process component, such as a flow controller 658, responsive to commands from the corresponding slave processor 172.

One slave controller 140 - 147 may contain one or more servo controller and one or more interface controller coupled with respective ports of the slave processor 170 - 172 for permitting control and monitor capabilities of various component motors and processing components from a single slave controller.

Alternatively, a servo controller and interface controller may each contain an onboard processor for improving the speed of processing and operation. Data provided by an encoder or process component to the servo controller or interface controller may be immediately processed by the on board processor which may also control a respective servo motor or processing component responsive to the data. In such a configuration, the slave processor may transfer the data from the interface processor or servo controller processor to the respective master controller and grand master controller.

CONVEYOR CONTROL SUBSYSTEM

The conveyor control subsystem 113 for controlling and monitoring the operation of the wafer conveyor 60 and the wafer transport units 62a, 62b or 562a, 562b or 544a, 544b therein is shown in Fig. 29. In general, a slave controller 143 of conveyor control 113 is coupled with drive actuator 71 for controllably moving and monitoring a wafer transport unit 62a along the guide 66. Further, slave controller 143 may operate transfer arm assembly 86 of the wafer transport unit 62a or 562a or 544a and the transferring of semiconductor wafers thereby. Similarly, slave controller 144 may be configured to operate wafer transport unit 62b or 562b or 544b and drive actuator 74.

The interfacing of slave controller 143 and light detector 91, drive actuator 71, linear

encoder 196 and wafer transport unit 62a is shown in detail in Fig. 36. The slave processor 171 of slave controller 143 is preferably coupled with a servo controller 176. Slave processor 171 may control the linear position of wafer transport unit 62a by operating drive actuator 71 via servo controller 176. Light detector 91 may provide linear position information of the wafer transport unit 62a along guide 66. Additionally, a linear encoder 196 may also be utilized for precisely monitoring the position of wafer transport unit 62 along guide 66.

The conveyor slave processor 171 may also control and monitor the operation of the transfer arm assembly 86 of the corresponding wafer transport unit 62a. Specifically, the conveyor processor 171 may be coupled with a transfer arm motor 194 within shaft 83 for controllably rotating the first and second arm extensions 87, 88. An incremental transfer arm rotation encoder 197 may be provided within the shaft 83 of each wafer transport unit 62a for monitoring the rotation of transfer arm assembly 86 and providing rotation data thereof to servo controller 176 and slave processor 171.

Slave controller 143 may be advantageously coupled with transfer arm elevation motor 195 within elevator 90 for controlling the elevational position of the transfer arm assembly 86. An incremental transfer arm elevation encoder 198 may be provided within the transfer arm elevator assembly 90 for monitoring the elevation of the transfer arm assembly 86.

In addition, conveyor slave controller 143 may be coupled with an air supply control valve actuator (not shown) via an interface controller for controlling a vacuum within wafer support 89 for selectively supporting a semiconductor wafer thereon.

Absolute encoders 199 may be provided within the wafer conveyor 60, interface modules 38, 39 and processing modules 19 to detect extreme conditions of operation and

protect servo motors therein. For example, absolute encoder 199 may detect a condition where the transfer arm assembly 86 has reached a maximum height and absolute encoder 199 may turn off elevator 90 to protect transfer arm elevator motor 195.

A similar approach may be used for the fiber optic signal communication system of the second and third embodiments of the wafer transfer units 562a, 562b and 544a, 544b, respectively. Particular, encoder 591 located in the elevator 590, encoder 592 located in the base motor 593 of the shaft 583, encoder 594 located in the shaft 583, wrist absolute encoder 595 located at the distal end of transfer arm assembly 586 and elbow absolute encoder 597 located at the base of the shaft 583 provide the rotational input of rotational encoder 193 of Fig. 35. Likewise, lift absolute encoder 596 located along the base motor 593, linear encoder 598, head rail encoder 599 and track CDD array absolute encoder 541 provide inputs for the lift encoder 192 and absolute encoder 199 of Fig. 35, respectively.

PROCESSING MODULE CONTROL

The control system 100 preferably includes a processing module control subsystem 114 - 116 corresponding to each wafer processing module 20, 22, 24 within the processing tool 10 according to the present disclosure. The control system 100 may also include additional processing module control subsystem 119 for controlling and/or monitoring additional wafer processing modules 19.

Respective processing module controls 114, 115, 116 may control and monitor the transferring of semiconductor wafers W between a corresponding wafer holder 810 and wafer transport unit 62a, 62b or 562a, 562b or 544a, 544b. Further, processing module controls

114, 115, 116 may advantageously control and/or monitor the processing of the semiconductor wafers W within each processing module 20, 22, 24.

Referring to Fig. 30, a single slave controller 147 may operate a plurality of wafer holders 401c-401e within a processing module 20. Alternatively, a single slave controller 145, 146 may operate and monitor a single respective wafer holder 401a, 401b. An additional slave controller 148 may be utilized to operate and monitor all process components 184 (*i.e.*, flow sensors, valve actuators, heaters, temperature sensors) within a single processing module 19. Further, as shown in Fig. 37, a single slave controller 145 may operate and monitor a wafer holder 410 and process components 184.

In addition, a single slave controller 145 - 148 may be configured to operate and monitor one or more wafer holder 401 and processing components 184. The interfacing of a slave controller 145 to both a wafer holder 401 and process components are shown in the control system embodiment in Fig. 37. In particular, a servo controller 177 and interface controller 180 may be coupled with respective ports connected to slave processor 172 of slave controller 145. Slave processor 172 may operate and monitor a plurality of wafer holder components via servo controller 177. In particular, slave processor 172 may operate lift motor 427 for raising operator arm 407 about lift drive shaft 456. An incremental lift motion encoder 455 may be provided within a wafer holder 401 to provide rotational information of lift arm 407 to the respective slave processor 172 or a processor within servo controller 177. Slave processor 172 may also control a rotate motor 428 within wafer holder 401 for rotating a processing head 406 about shafts 429, 430 between a process position and a semiconductor wafer transfer position. Incremental rotate encoder 435 may provide rotational information

regarding the processing head 406 to the corresponding slave processor 172.

Spin motor 480 may also be controlled by a processor within servo controller 177 or slave processor 172 for rotating the wafer holder 478 during processing of a semiconductor wafer W held thereby. An incremental spin encoder 498 is preferably provided to monitor the rate of revolutions of the wafer holder 478 and supply the rate information to the slave processor 172.

Plating module control 114 advantageously operates the fingertips 414 of the wafer holder 478 for grasping or releasing a semiconductor wafer. In particular, slave processor 172 may operate a valve via pneumatic valve actuator 201 for supplying air to pneumatic piston 502 for actuating fingertips 414 for grasping a semiconductor wafer. The slave controller 145 within the plating module control 114 may thereafter operate the valve actuator 201 to remove the air supply thereby disengaging the fingertips 414 from the semiconductor wafer. Slave processor 172 may also control the application of electrical current through the finger assembly 824 during the processing of a semiconductor wafer by operating relay 202.

The processing module controls 114, 115, 116 preferably operate and monitor the processing of semiconductor wafers within the corresponding wafer processing modules 20, 22, 24 via instrumentation or process components 184.

Referring to Fig. 33, the control operation for the plating processing module 20 is described. Generally, slave processor 172 monitors and/or controls process components 184 via interface controller 180. Slave processor 172 within the plating module control 114 operates pump 605 to draw processing solution from the process fluid reservoir 604 to the pump discharge filter 607. The processing fluid passes through the filter, into supply manifold

652 and is delivered via bowl supply lines to a plurality of processing plating bowls wherein the semiconductor wafers are processed. Each bowl supply line preferably includes a flow sensor 657 coupled with the plating processing module control 114 for providing flow information of the processing fluid thereto. Responsive to the flow information, the slave processor 172 may operate an actuator of flow controller 658 within each bowl supply line to control the flow of processing fluid therethrough. Slave processor 172 may also monitor and control a back pressure regulator 656 for maintaining a predetermined pressure level within the supply manifold 652. The pressure regulator 656 may provide pressure information to the slave processor 172 within the plating processing control module 114.

Similarly, processing module control subsystems 115, 116 may be configured to control the processing of semiconductor wafers within the corresponding prewet module 22 and resist module 24.

INTERFACE MODULE CONTROL

Each interface module control subsystem 110 preferably controls and monitors the operation of wafer interface modules 38, 39. More specifically, interface module control 110 controls and monitors the operation of the wafer cassette turnstiles 40, 41 and elevators 42, 43 of respective semiconductor wafer interface modules 38, 39 to exchange wafer cassettes 16.

Slave processor 170 within slave controller 140 of interface module control 110 may operate and monitor the function of the interface modules 38, 39. In particular, slave processor 170 may operate doors 35, 36 for providing access into the processing tool 10 via ports 32, 33. Alternatively, master control 100 may operate doors 35, 36.

Referring to Fig. 31, an embodiment of the interface module control portion for controlling wafer interface module 38 is discussed. In particular, the slave processor 170 is coupled with servo controller 175. Either slave processor 170 or a processor on board servo controller 175 may operate the components of interface module 38. In particular, slave processor 170 may control turnstile motor 185 for operating rotate functions of turnstile 40 moving wafer cassettes 16 between a load position and a transfer position. Incremental turnstile encoder 190 monitors the position of turnstile 40 and provides position data to slave processor 170. Alternatively, servo controller 175 may include a processor for reading information from turnstile encoder 190 and controlling turnstile motor 185 in response thereto. Servo controller 175 may alert slave processor 170 once turnstile 40 has reaches a desired position.

Each wafer cassette turnstile 40 includes a motor for controlling the positioning of saddles 45, 46 connected thereto. The slave processor 170 may control the position of saddles 45, 46 through operation of the appropriate saddle motor 186 to orient wafer cassettes 16 attached thereto in one of a vertical and horizontal orientation. Incremental saddle encoders 191 are preferably provided within each wafer cassette turnstile 40 for providing position information of the saddles 45, 46 to the respective slave processor 170.

Either slave processor 170 or servo controller 175 may be configured to control the operation of the wafer cassette elevator 42 for transferring a wafer cassette 16 between either the exchange position and the extraction position. The slave processor 170 may be coupled with an elevator lift motor 187 and elevator rotation motor 188 for controlling the elevation and rotation of elevator 42 and elevator support 47. Incremental lift encoder 192 and

incremental rotation encoder 193 may supply elevation and rotation information of the elevator 42 and support 47 to slave processor 170.

Absolute encoders 199 may be utilized to notify slave processor of extreme conditions such as when elevator support 47 reaches a maximum height. Elevator lift motor 187 may be shut down in response to the presence of an extreme condition by absolute encoder 199.

WAFER CASSETTE TRAY

A wafer cassette tray 50 for holding a wafer cassette 16 is shown in detail in Fig. 9. Each cassette tray 50 may include a base 51 and an upright portion 54 preferably perpendicular to the base 51. Two lateral supports 52 may be formed on opposing sides of the base 51 and extend upward therefrom. Lateral supports 52 assist with maintaining wafer cassettes 16 thereon in a fixed position during the movement, rotation and exchange of wafer cassettes 16. Each lateral support 52 contains a groove 53 preferably extending the length thereof configured to engage with the forks of saddles 45, 46.

The wafer cassette trays 50 are preferably utilized during the handling of wafer cassettes 16 within the wafer cassette interface modules 38, 39 where the wafer cassettes 16 are transferred from a load position to an extraction position providing access of the semiconductor wafers W to wafer transport units 62, 64 within the conveyor 60.

ELECTROPLATING STATION

Fig. 33 shows principal components of a second semiconductor processing station 900 is specifically adapted and constructed to serve as an electroplating station. The two principal parts of processing station 900 are the wafer rotor assembly, shown generally at 906, and the electroplating bowl assembly 303.

ELECTROPLATING BOWL ASSEMBLY 303

Fig. 33 shows an electroplating bowl assembly 303. The process bowl assembly consists of a process bowl or plating vessel 316 having an outer bowl side wall 317, bowl bottom 319, and bowl rim assembly 917. The process bowl is preferably circular in horizontal cross-section and generally cylindrical in shape although other shapes may be possible.

The bowl assembly 303 includes a cup assembly 320 which is disposed within a process bowl vessel 317. Cup assembly 320 includes a fluid cup portion 321 holding the chemistry for the electroplating process. The cup assembly also has a depending skirt 371 which extends below the cup bottom 323 and may have flutes open therethrough for fluid communication and release of any gas that might collect as the chamber below fills with liquid. The cup is preferably made from polypropylene or other suitable material.

A lower opening in the bottom wall of the cup assembly 320 is connected to a polypropylene riser tube 330 which is adjustable in height relative thereto by a threaded connection. A first end of the riser tube 330 is secured to the rear portion of an anode shield 393 which supports anode 334. A fluid inlet line 325 is disposed within the riser tube 330. Both the riser tube 330 and the fluid inlet line are secured with the processing bowl assembly 303 by a fitting 362. The fitting 362 can accommodate height adjustment of both the riser tube and line 325. As such, the connection between the fitting 362 and the riser tube 330 facilitates vertical

adjustment of the anode position. The inlet line 325 is preferably made from a conductive material, such as titanium, and is used to conduct electrical current to the anode 324, as well as supply fluid to the cup.

Process fluid is provided to the cup through fluid inlet line 325 and proceeds therefrom through fluid inlet openings 324. Plating fluid then fills the chamber 904 through opening 324 as supplied by a plating fluid pump (not shown) or other suitable supply.

The upper edge of the cup side wall 322 forms a weir which limits the level of electroplating solution within the cup. This level is chosen so that only the bottom surface of wafer W is contacted by the electroplating solution. Excess solution pours over this top edge surface into an overflow chamber 345. The level of fluid in the chamber 345 is preferably maintained within a desired range for stability of operation by monitoring the fluid level with appropriate sensors and actuators. This can be done using several different outflow configurations. A preferred configuration is to sense a high level condition using an appropriate sensor and then drain fluid through a drain line as controlled by a control valve. It is also possible to use a standpipe arrangement (not illustrated). and such is used as a final overflow protection device in the preferred plating station. More complex level controls are also possible.

The outflow liquid from chamber 345 is preferably returned to a suitable reservoir. The liquid can then be treated with additional plating chemicals or other constituents of the plating or other process liquid and used again.

In the preferred uses according to this invention. the anode 334 is a consumable anode used in connection with the plating of copper or other metals onto semiconductor materials. The specific anode will vary depending upon the metal being plated and other specifics of the plating liquid being used. A number of different consumable anodes which are commercially available

may be used as anode 334.

Fig. 33 also shows a diffusion plate 375 provided above the anode 334 for providing a more even distribution of the fluid plating bath across the Wafer W. Fluid passages are provided over all or a portion of the diffusion plate 375 to allow fluid communication therethrough. The height of the diffusion plate is adjustable using diffuser height adjustment mechanisms 386.

The anode shield 393 is secured to the underside of the consumable anode 334 using anode shield fasteners 394 to prevent direct impingement by the plating solution as the solution passes into the processing chamber 904. The anode shield 393 and anode shield fasteners 394 are preferably made from a dielectric material, such as polyvinylidene fluoride or polypropylene. The anode shield is advantageously about 2-5 millimeters thick, more preferably about 3 millimeters thick.

The anode shield serves to electrically isolate and physically protect the back side of the anode. It also reduces the consumption of organic plating liquid additives. Although the exact mechanism may not be known at this time, the anode shield is believed to prevent disruption of certain materials which develop over time on the back side of the anode. If the anode is left unshielded, the organic chemical plating additives are consumed at a significantly greater rate. With the shield in place, these additives are not consumed as quickly.

WAFER ROTOR ASSEMBLY

The wafer rotor assembly 906 holds a wafer W for rotation within the processing chamber 904. The wafer rotor assembly 906 includes a rotor assembly 984 having a plurality of wafer-engaging fingers 979 that hold the wafer against features of the rotor. Fingers 979 are preferably adapted to conduct current between the wafer and a plating electrical power supply and may be constructed in accordance with various configurations to act as current thieves.

The various components used to spin the rotor assembly 984 are disposed in a fixed housing 970. The fixed housing is connected to a horizontally extending arm 909 that, in turn, is connected to a vertically extending arm. Together, the arms 908 and 909 allow the assembly 906 to be lifted and rotated from engagement with the bowl assembly to thereby present the wafer to the wafer conveying assembly 60for transfer to a subsequent processing station.

Numerous modifications may be made to the foregoing system without departing from the basic teachings thereof. Although the present invention has been described in substantial detail with reference to one or more specific embodiments, those of skill in the art will recognize that changes may be made thereto without departing from the scope and spirit of the invention as set forth in the appended claims.

CLAIMS

What is Claimed is:

1. A transport system for manipulating a semiconductor wafer within a processing section of a processing apparatus, the transport system comprising:

a transport unit guide disposed within the processing apparatus for supporting a wafer transfer unit as it moves between a first position and a second position, the transport unit guide comprising a frame, a lateral guide rail mounted on the frame and a series of magnetic segments arranged upon the transport unit guide proximate the lateral guide rail;

the wafer transfer unit comprising a tram translatably attached to the lateral guide rail, a wafer transfer arm assembly for manipulating the semiconductor wafer, an electromagnet mounted on the tram in cooperative relation with the magnetic segments for moving the transfer unit along the guide rail, actuators responsive to control signals for controlling the position of the transfer unit and transfer arm assembly, sensors for monitoring the position of the transfer unit and the transfer arm assembly;

a controller disposed remote of the transfer unit, the controller being responsive to signals received from the sensors and providing the control signals to the actuators for directing the movement of the transfer unit and transfer arm assembly; and

a communication link between the wafer transfer unit and the controller for facilitating control of the operation of the wafer transfer unit.

2. A transport system as claimed in claim 1 wherein the communication link between the wafer transfer unit and the controller is an optical communication link.

3. A transport system as claimed in claim 2 wherein the optical communications link comprises one or more fiber-optic lines extending between the wafer transfer unit and the controller.

4. A transport system as claimed in claim 1 and further comprising:

a further lateral guide rail mounted on the frame and disposed parallel with and vertically below the lateral guide rail;

the tram being translatably attached to the further lateral guide rail.

5. A transport system as claimed in claim 1 and further comprising an angular adjustment mechanism for adjusting the angular orientation of the wafer transfer arm assembly with respect to the tram.

6. A transport system as claimed in claim 4 and further comprising an angular adjustment mechanism for adjusting the angular orientation of the wafer transfer arm assembly with respect to the tram.

7. A transport system as claimed in claim 4 wherein the tram is attached to the lateral guide rail and the further lateral guide rail with respective compliant mounting assemblies.

8. A semiconductor wafer processing apparatus, comprising:

a wafer conveyor system including

a central support extending along a linear transfer path,

a first wafer transport unit disposed on a first side of the central support and mounted thereto for translational movement along the linear transfer path,

a second wafer transport unit disposed on a second side of the central support and mounted thereto for translational movement parallel to the first transport unit along the linear transfer path;

a plurality of wafer processing modules adjacent opposing sides of said wafer conveyor system; and

said first and second wafer transport units adapted to respectively support an individual semiconductor wafer and to access each of said wafer processing modules for transferring semiconductor wafers therebetween.

9. The semiconductor wafer processing apparatus of claim 8 wherein said first and second wafer transport units are removed along the transfer path using respective linear magnetic motors.

10. The semiconductor wafer processing apparatus of claim 8 herein each said at least one wafer transport unit includes:

a tram;

a wafer transfer arm connected to said tram for 2 degree movement in a generally horizontal plane, the wafer transfer arm having a vacuum support mounted at a distal end thereof for holding a semiconductor wafer;

a transfer arm elevator for adjusting the vertical position of said wafer transfer arm with respect to said tram.

11. The semiconductor wafer processing apparatus of claim 8 wherein each of said first and second wafer transport units includes a position sensor for determining the position of the respective wafer transport unit relative to said wafer processing modules.

12. The semiconductor wafer processing apparatus of claim 8 and further comprising:

at least one wafer interface module adjacent said wafer conveyor for supporting a wafer cassette having a plurality of semiconductor wafers therein;

said wafer interface configured to present said wafer cassette in an extraction position to permit at least one of said first and second wafer transport units to access the semiconductor wafers in total wafer cassettes for.

13. The semiconductor wafer processing apparatus of claim 12 are wherein each said at least one wafer interface includes:

a wafer cassette turnstile for moving a wafer cassette between a load position and a transfer position;

a wafer cassette elevator adjacent said wafer cassette turnstile and configured to transfer wafer cassettes therebetween and provide the wafer cassette in the extraction position.

14. The semiconductor wafer processing apparatus of claim 12 wherein said semiconductor wafer processing apparatus further comprises a cassette loading door adjacent said at least one wafer interface module and being configured to permit wafer cassettes to pass therethrough.

15. The semiconductor wafer processing apparatus of claim 8 further comprising:

a first wafer interface module for receiving wafer cassettes containing unprocessed semiconductor wafers, the first wafer interface module presenting the unprocessed semiconductor wafers to the wafer transfer assembly in a generally horizontal extraction position;

a second wafer interface module for receiving processed semiconductor wafers into a wafer cassettes from below wafer transfer assembly, the second wafer interface module accepting the processed semiconductor wafers from the wafer transfer assembly in a generally horizontal insertion position.

16. The semiconductor wafer processing apparatus of claim 8 wherein the central support comprises:

a frame;

a first set of magnetic segments in fixed relationship with respect to the frame along a first side thereof along the length of the linear path;

a second set of magnetic segments in fixed relationship with respect to the frame along a second side thereof along the length of the linear path;

first and second lateral guide rails mounted on opposite sides of the frame and supporting the first and second wafer transfer units respectively.

17. The semiconductor wafer processing apparatus of claim 16 wherein each of the first and second wafer transfer units comprises:

a tram translatably attached to the respective lateral guide rail;

an electromagnet mounted on the tram in cooperative relation with the respective magnetic segments for moving the wafer transfer unit along the respective guide rail;

a plurality of actuators responsive to control signals for controlling the position of the wafer transfer unit and transfer arm assembly;

a plurality of the sensors for monitoring the position of the transfer unit and the transfer arm assembly.

18. The semiconductor wafer processing apparatus of claim 8 and further comprising an air supply intermediate opposing ones of said wafer processing modules for supplying air to said semiconductor wafer processing apparatus.

19. The semiconductor wafer processing apparatus of claim 8 wherein said wafer conveyor system includes at least one exhaust duct adjacent thereto for removing air.

20. The semiconductor wafer processing apparatus of claim 8 wherein said wafer processing modules are interchangeable.

21. A semiconductor wafer processing apparatus, comprising:

a plurality of wafer processing modules for processing a semiconductor wafer, each of said wafer processing modules being interchangeable;

a wafer conveyor adjacent said wafer processing modules and having at least one wafer transport unit adapted for controlled movement along a generally linear transfer path;

said at least one wafer transport unit configured to support a semiconductor wafer and access each of said wafer processing modules for transferring semiconductor wafers therebetween.

22. The semiconductor wafer processing apparatus of claim 21 wherein said wafer conveyor moves said at least one wafer transport unit along the linear transfer path using a linear magnetic motor.

23. A method of handling semiconductor wafers within a semiconductor wafer processing apparatus having a plurality of wafer processing modules and a wafer conveyor adjacent thereto, comprising the steps of:

a. receiving at least one wafer cassette having a plurality of semiconductor wafers therein;

b. moving a first wafer transport unit along the wafer conveyor to transport a first individual wafer between one of the at least one wafer cassettes and a first one of the wafer processing modules;

c. moving a second wafer transport unit along the wafer conveyor to transport a second individual wafer between one of the at least one wafer cassettes and a second one of the wafer processing modules;

wherein said moving of the first wafer transport unit and said moving of the second wafer transport unit overlap in time.

24. The method of claim 23 and further comprising a step after step a of translating the at least one wafer cassette from a vertical orientation to a horizontal orientation so as to present semiconductor wafers contained therein in a generally horizontal orientation.

25. The method of claim 23 and further comprising the steps of:

storing wafer cassettes having unprocessed semiconductor wafers in the to and and in and and and and than in an and than than inward in a first interface module; and

storing wafer cassettes having processed semiconductor wafers in a second interface module.

26. A transport system for manipulating a semiconductor wafer within a processing section of a semiconductor processing apparatus, the transport system comprising:

a transport unit guide disposed within the processing apparatus for supporting a wafer transfer unit as it moves between a first position and a second position, the transport unit guide comprising a frame, a lateral guide rail mounted on the frame and a series of magnetic segments arranged upon the transport unit guide proximate the lateral guide rail;

the wafer transfer unit comprising a tram translatably attached to the lateral guide rail, a wafer transfer arm assembly for manipulating the semiconductor wafer, an electromagnet mounted on the tram in cooperative relation with the magnetic segments for moving the transfer unit along the guide rail; and

an angular adjustment mechanism for adjusting the angular orientation of the wafer transfer arm assembly with respect to the tram.

27. A transport system as claimed in claim 26 and further comprising:

a plurality of actuators responsive to control signals for controlling the position of the transfer unit and transfer arm assembly;

a plurality of sensors for monitoring the position of the transfer unit and the transfer arm assembly.

28. A transport system as claimed in claim 27 and further comprising:

a controller disposed remote of the transfer unit, the controller being responsive to signals received from the sensors and providing the control signals to the actuators for directing the movement of the transfer unit and transfer arm assembly; and

a communication link between the wafer transfer unit and the controller for facilitating control of the operation of the wafer transfer unit.

29. A transport system as claimed in claim 28 wherein the communication link between the wafer transfer unit and the controller is an optical communication link.

30. A transport system as claimed in claim 29 wherein the optical communications link comprises one or more fiber-optic lines extending between the wafer transfer unit and the controller.

31. A transport system as claimed in claim 26 for and further comprising:

a further lateral guide rail mounted on the frame and disposed parallel with and vertically below the lateral guide rail;

the tram being translatably attached to the further lateral guide rail.

32. A transport system as claimed in claim 31 wherein the tram is attached to the lateral guide rail and the further lateral guide rail with respective compliant mounting assemblies.

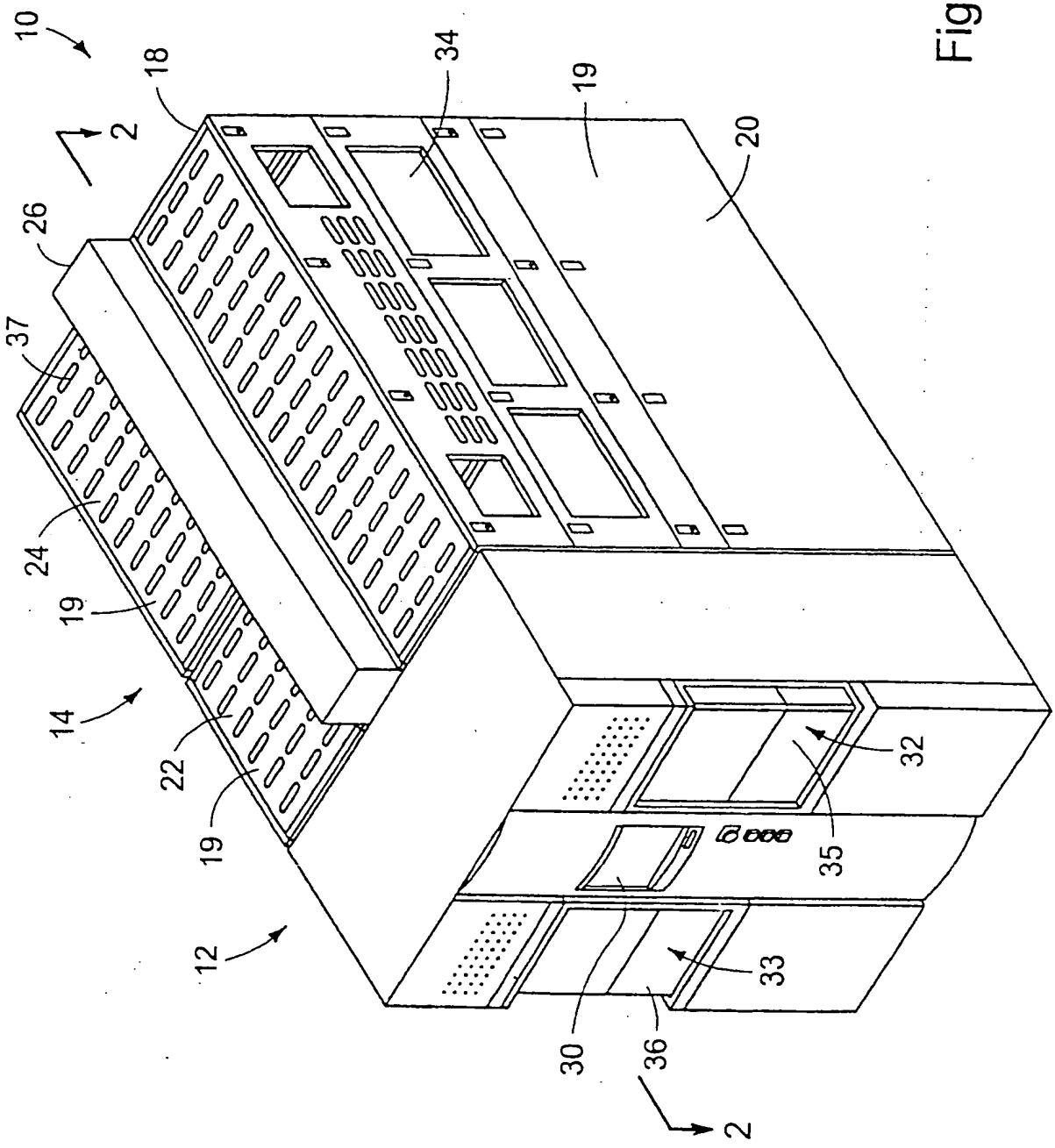
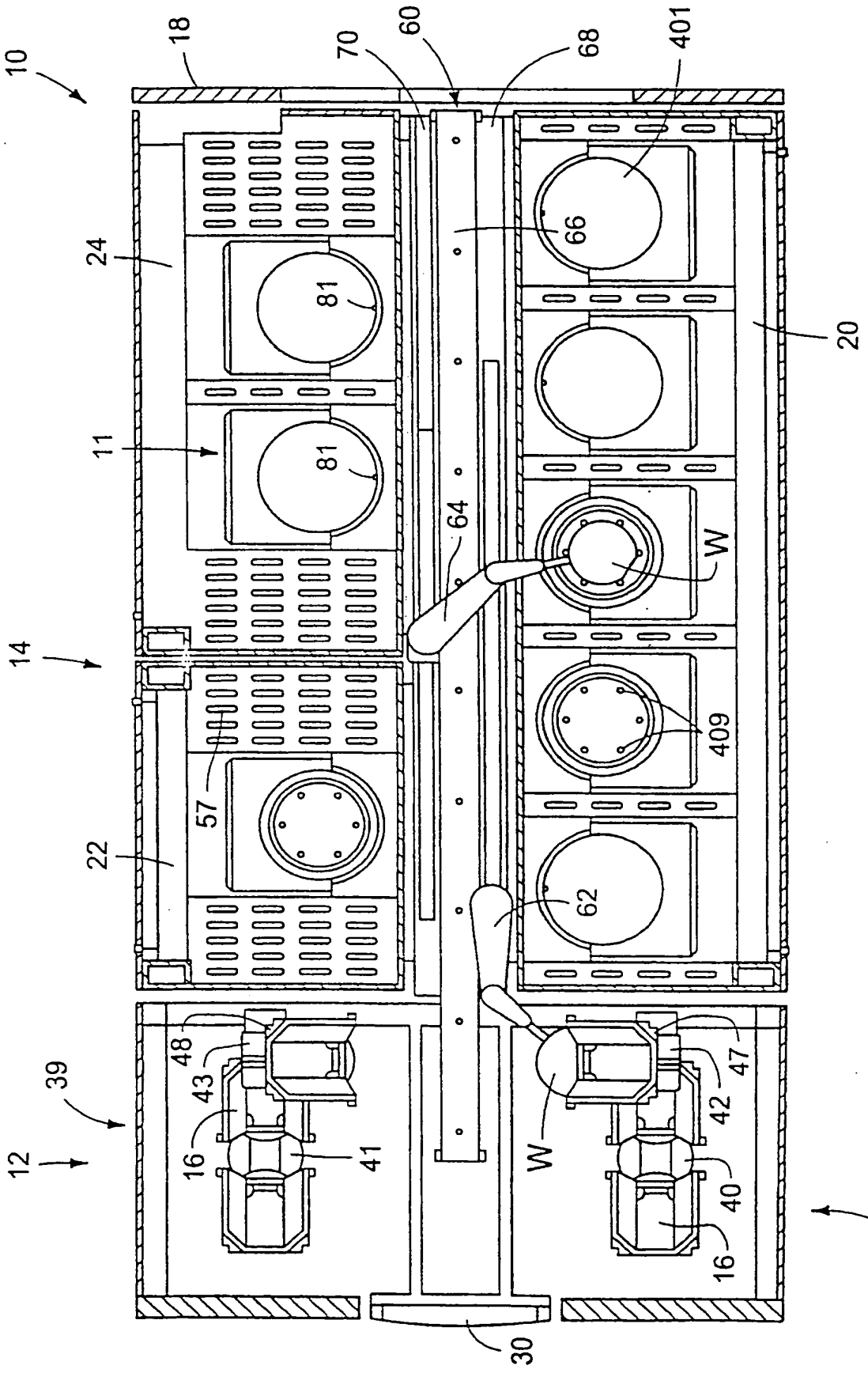


Fig. 1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401
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66
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81
64
W
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41
W
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16
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Fig. 2

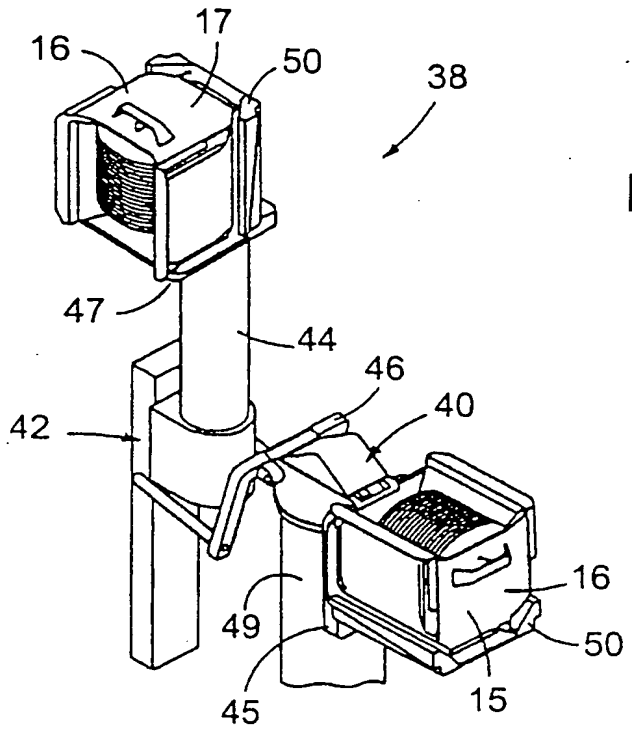
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Fig. 3

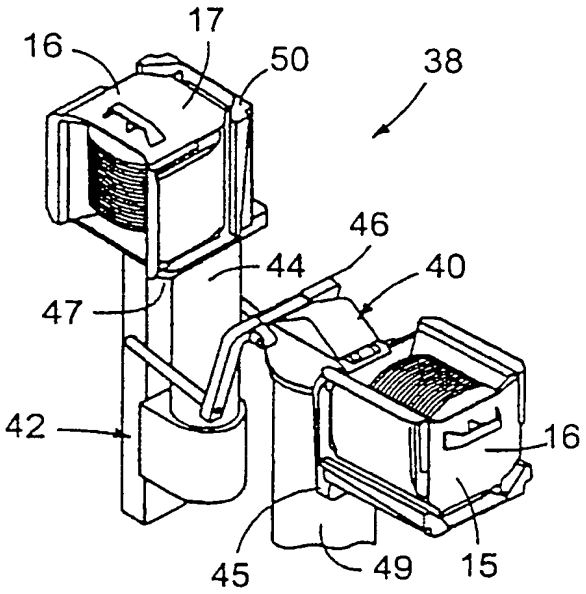
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Fig. 4

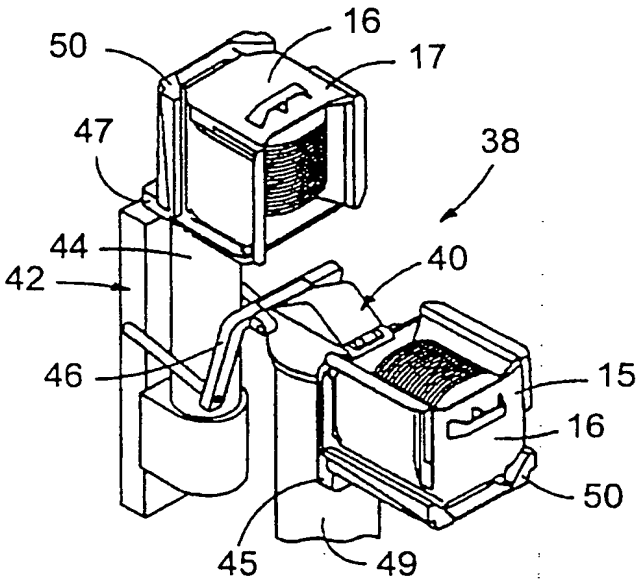
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Fig. 5

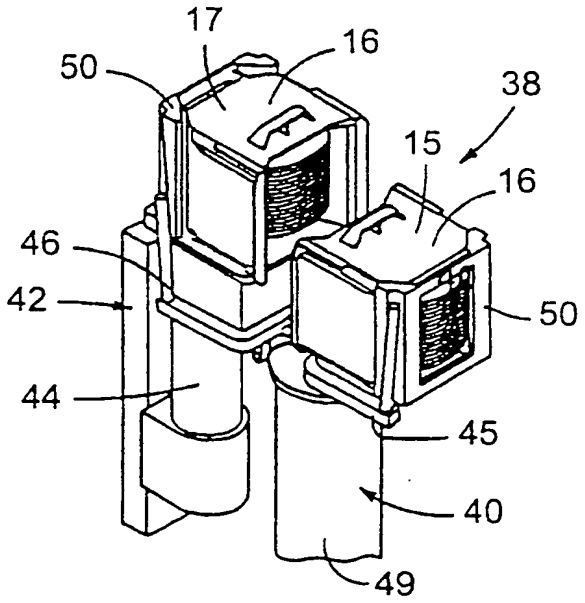
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Fig. 6

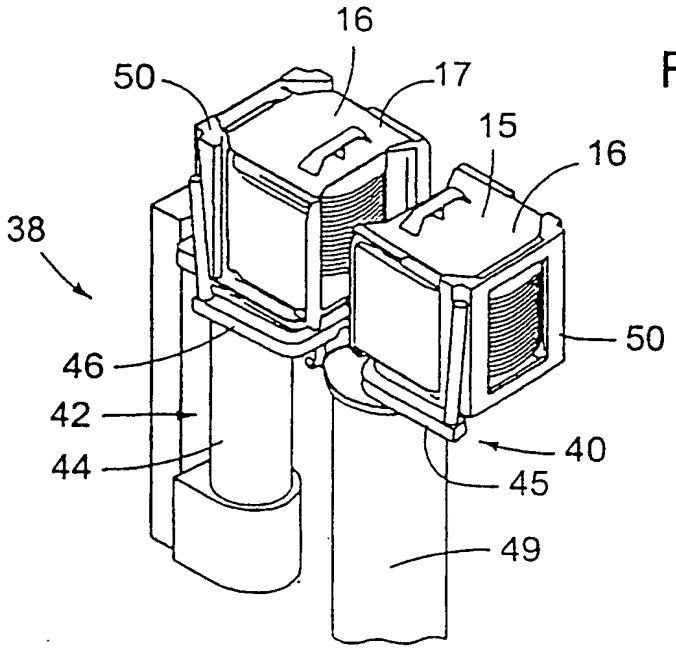
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Fig. 7

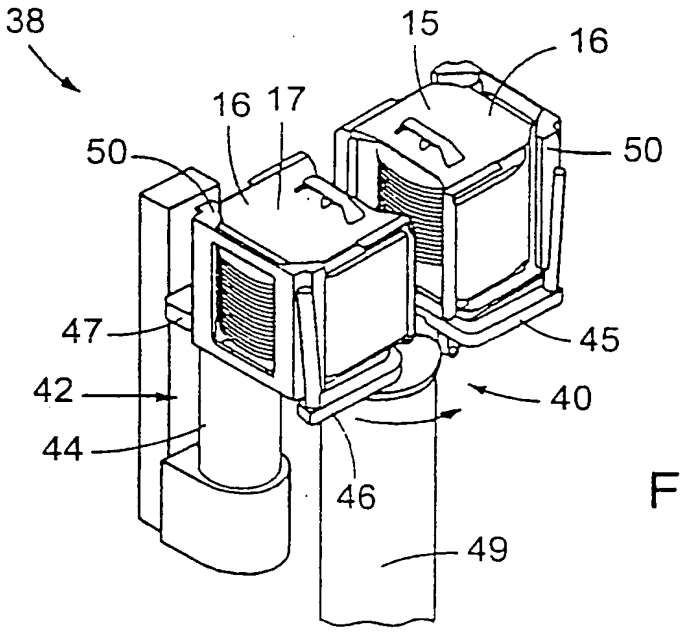
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Fig. 8

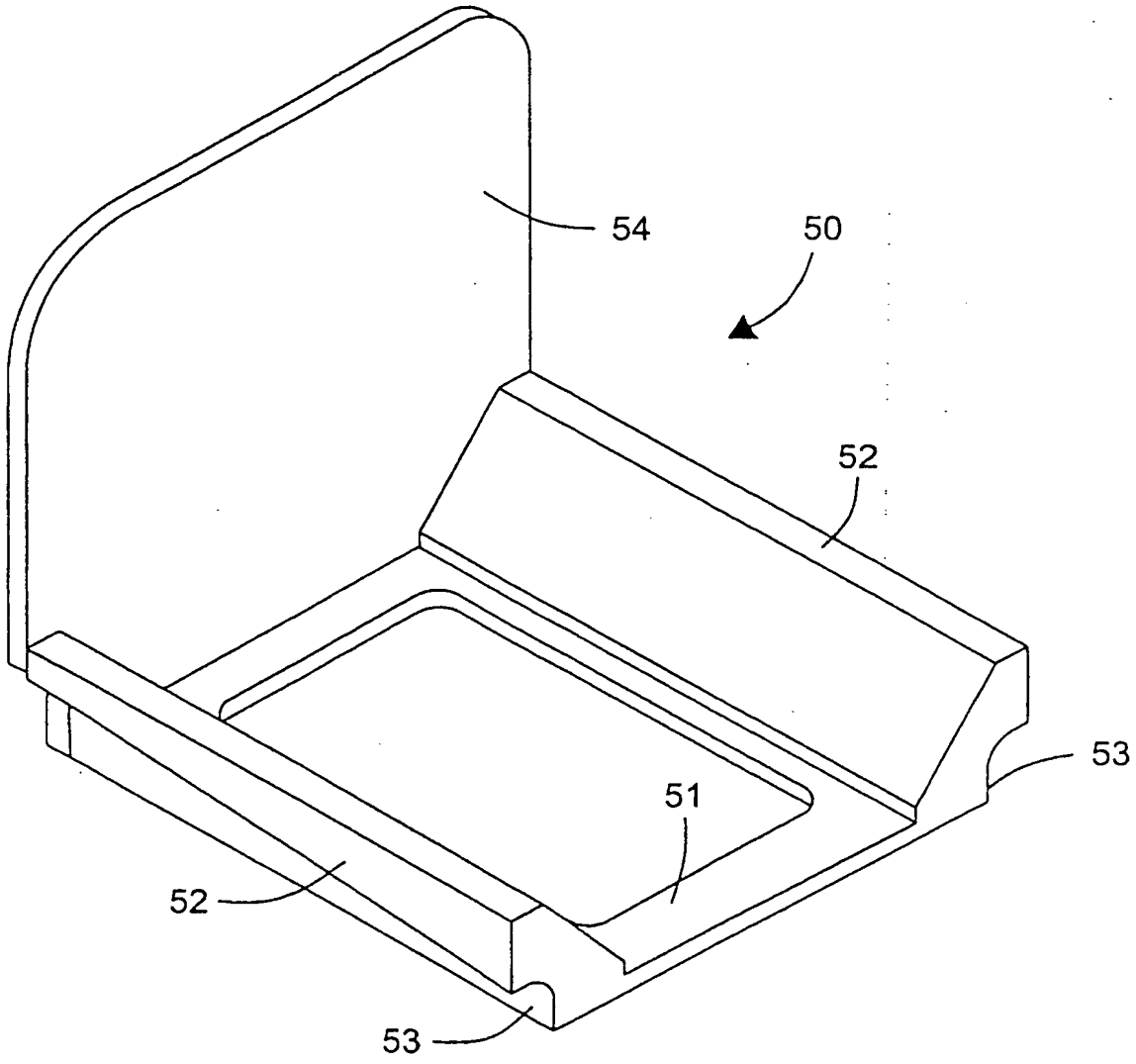


Fig. 9

Fig. 10

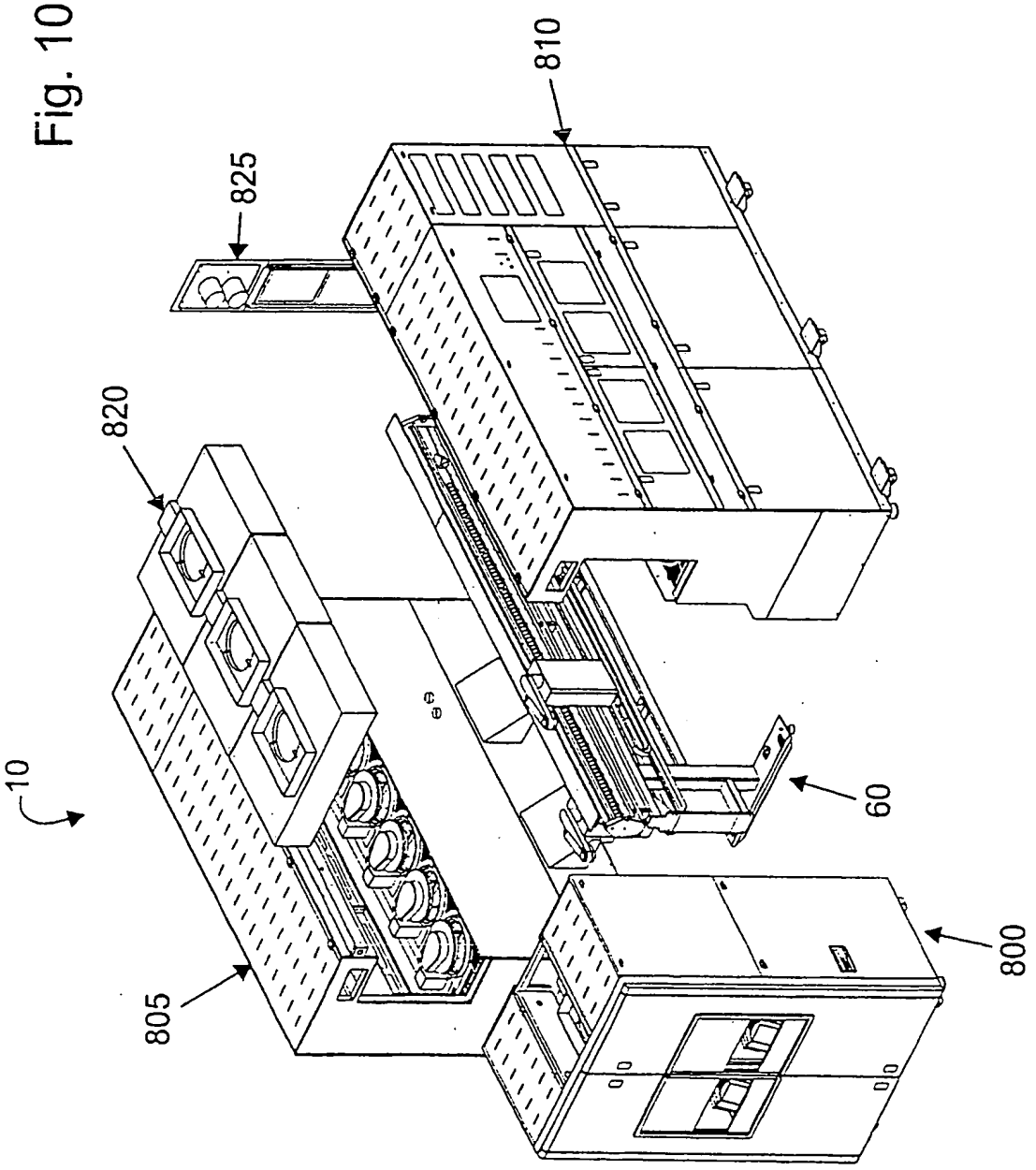


Fig. 11

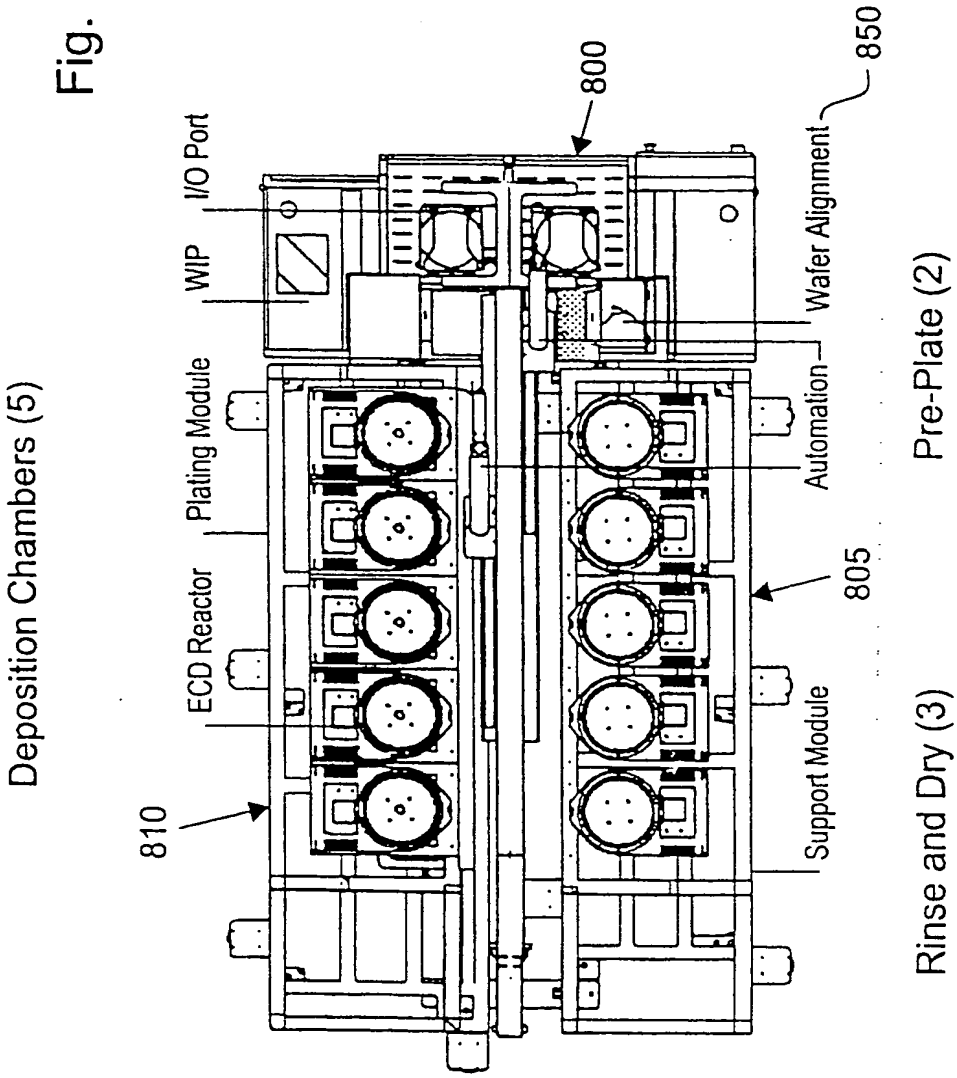

800
850
I/O Port
WIP
Plating Module
ECD Reactor
810
Wafer Alignment
Automation
805
Support Module
Deposition Chambers (5)
Pre-Plate (2)
Rinse and Dry (3)

Fig. 12

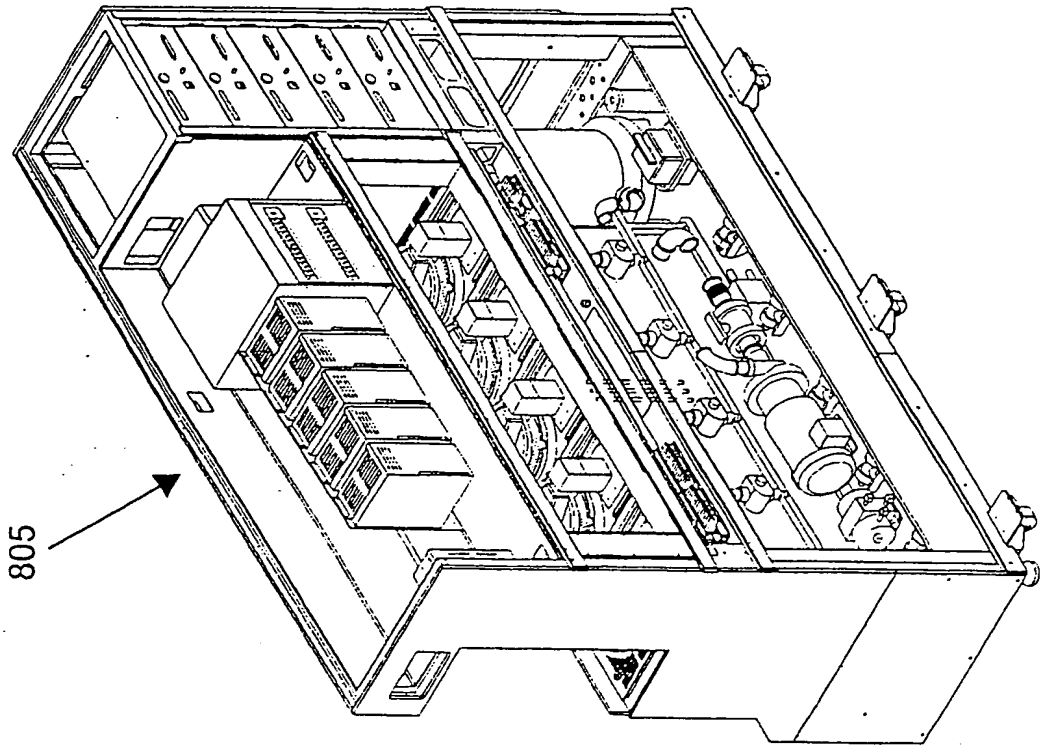


Fig. 13

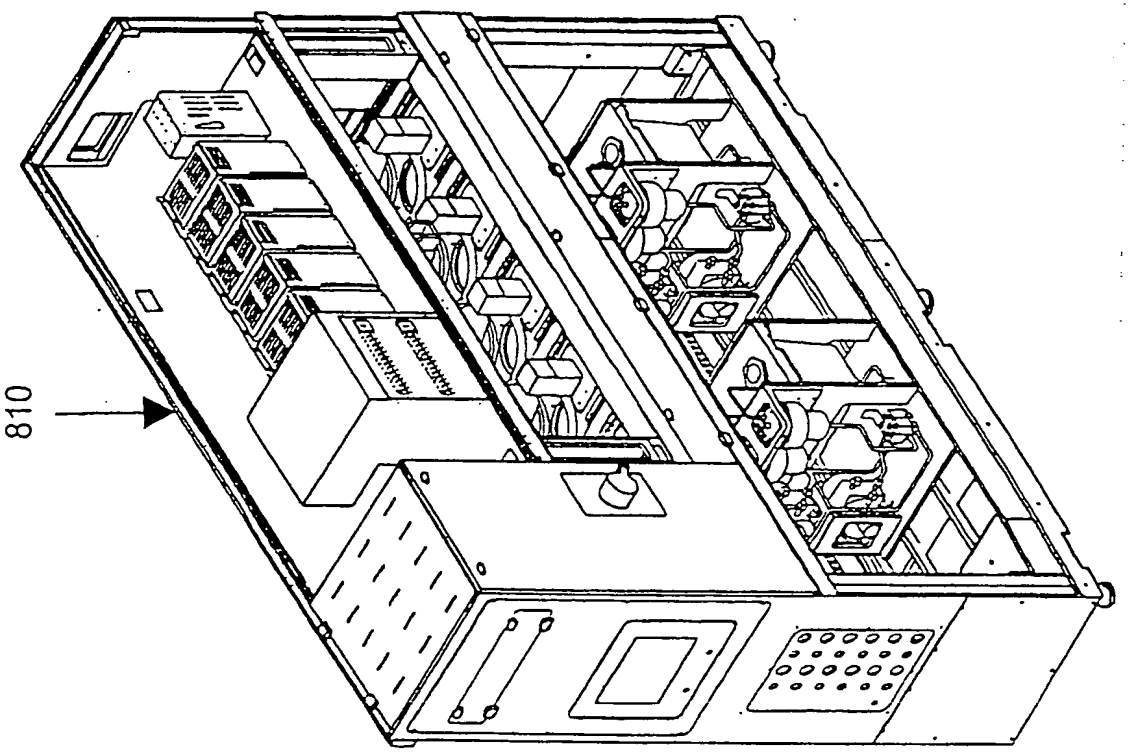


Fig. 14

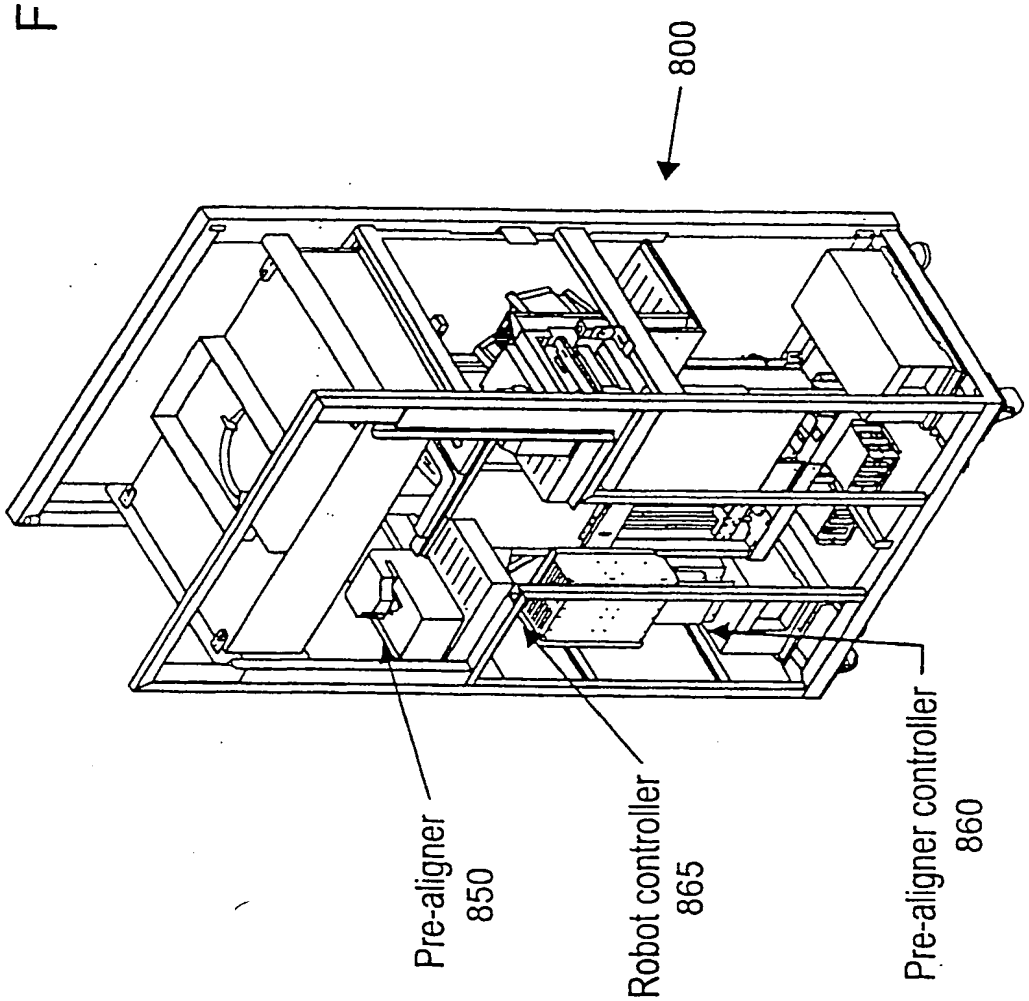
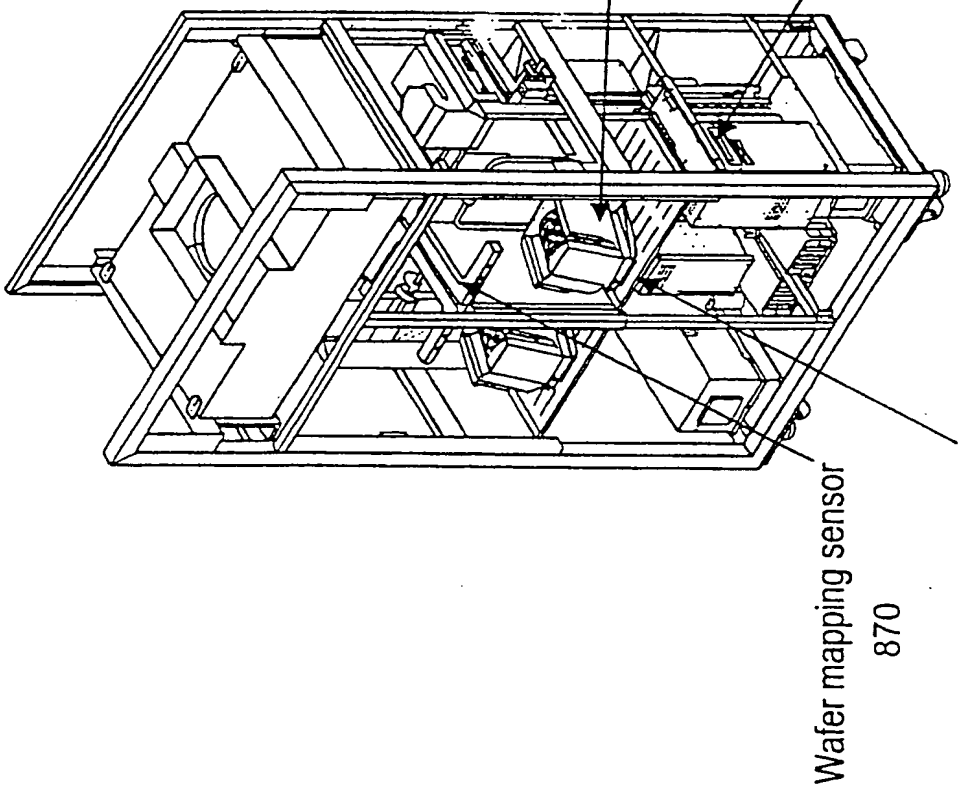

800
Pre-aligner
850
Robot controller
865
Pre-aligner controller
860

Fig. 15


Lift/tilt mechanism
System control computer
875
Wafer mapping sensor
870
4 axis controller
880

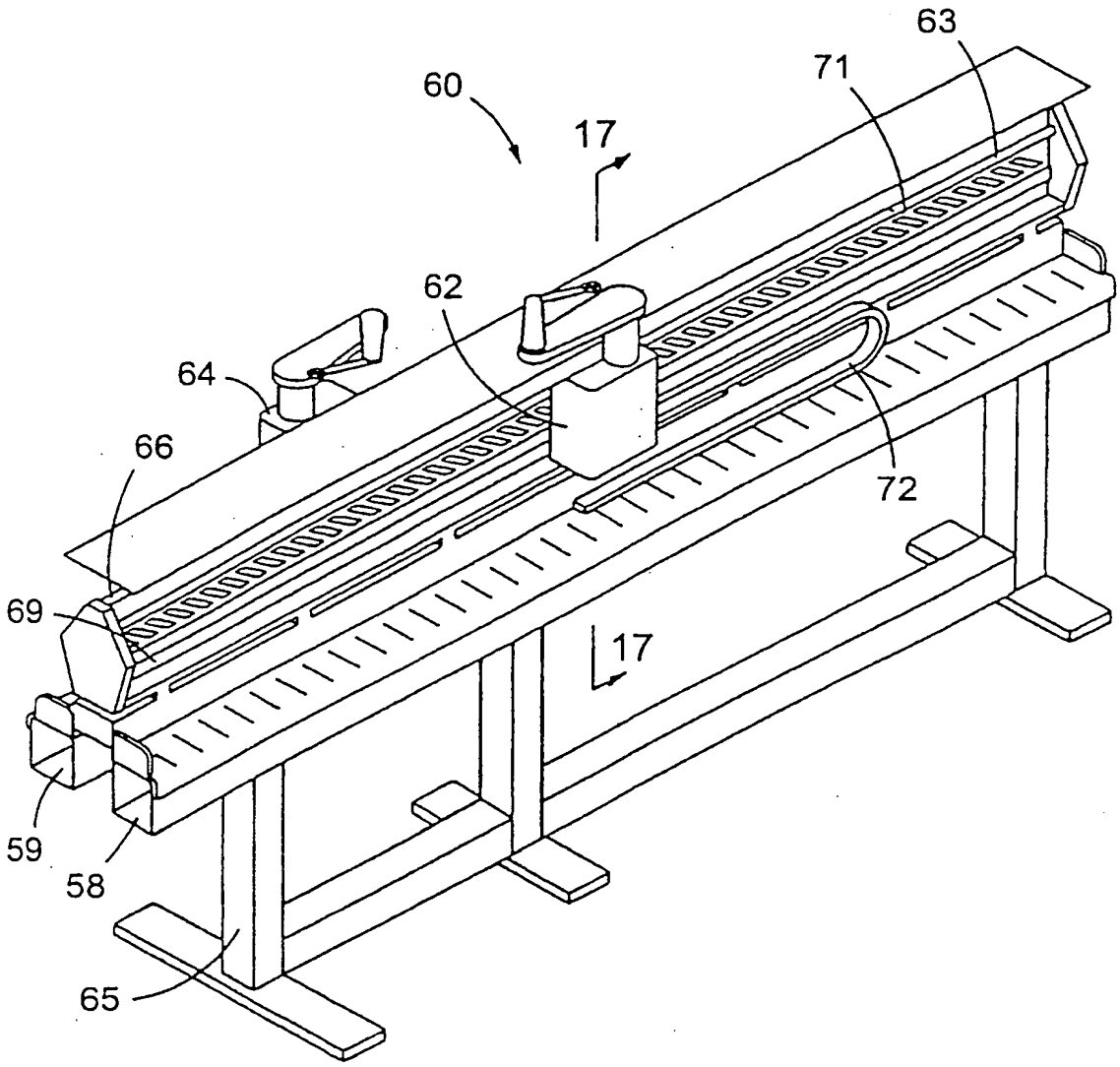


Fig. 16

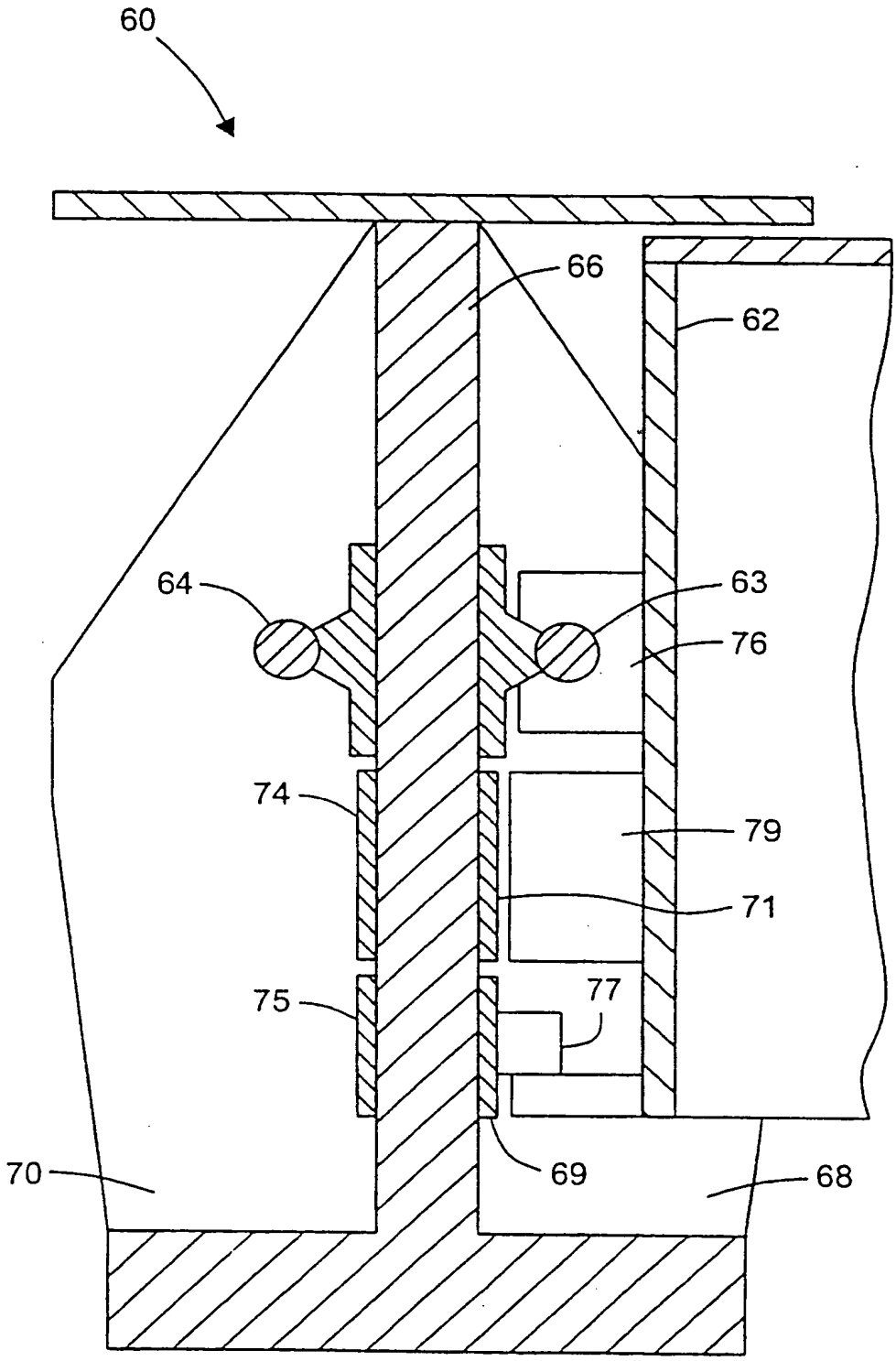


Fig. 17

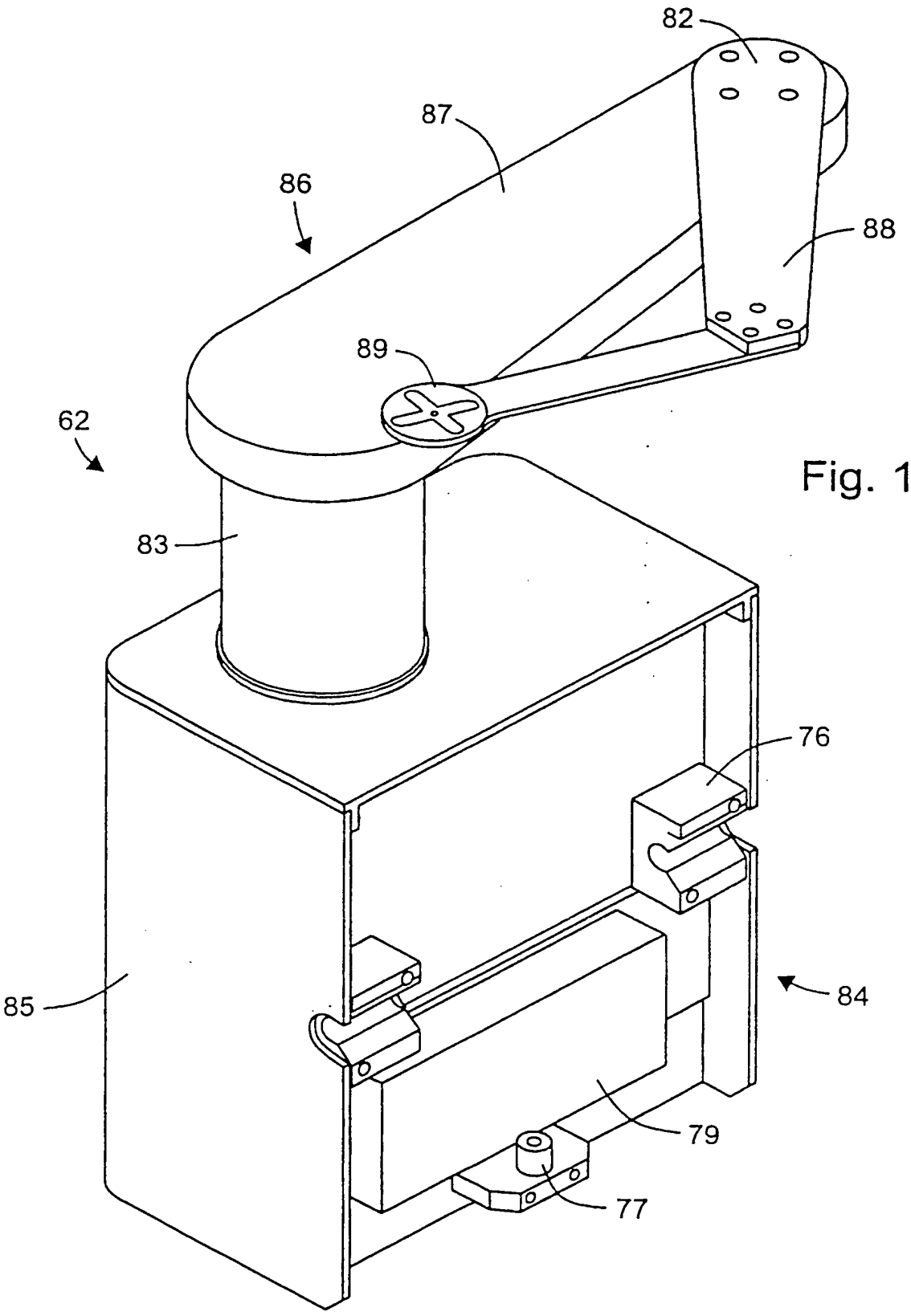


Fig. 18

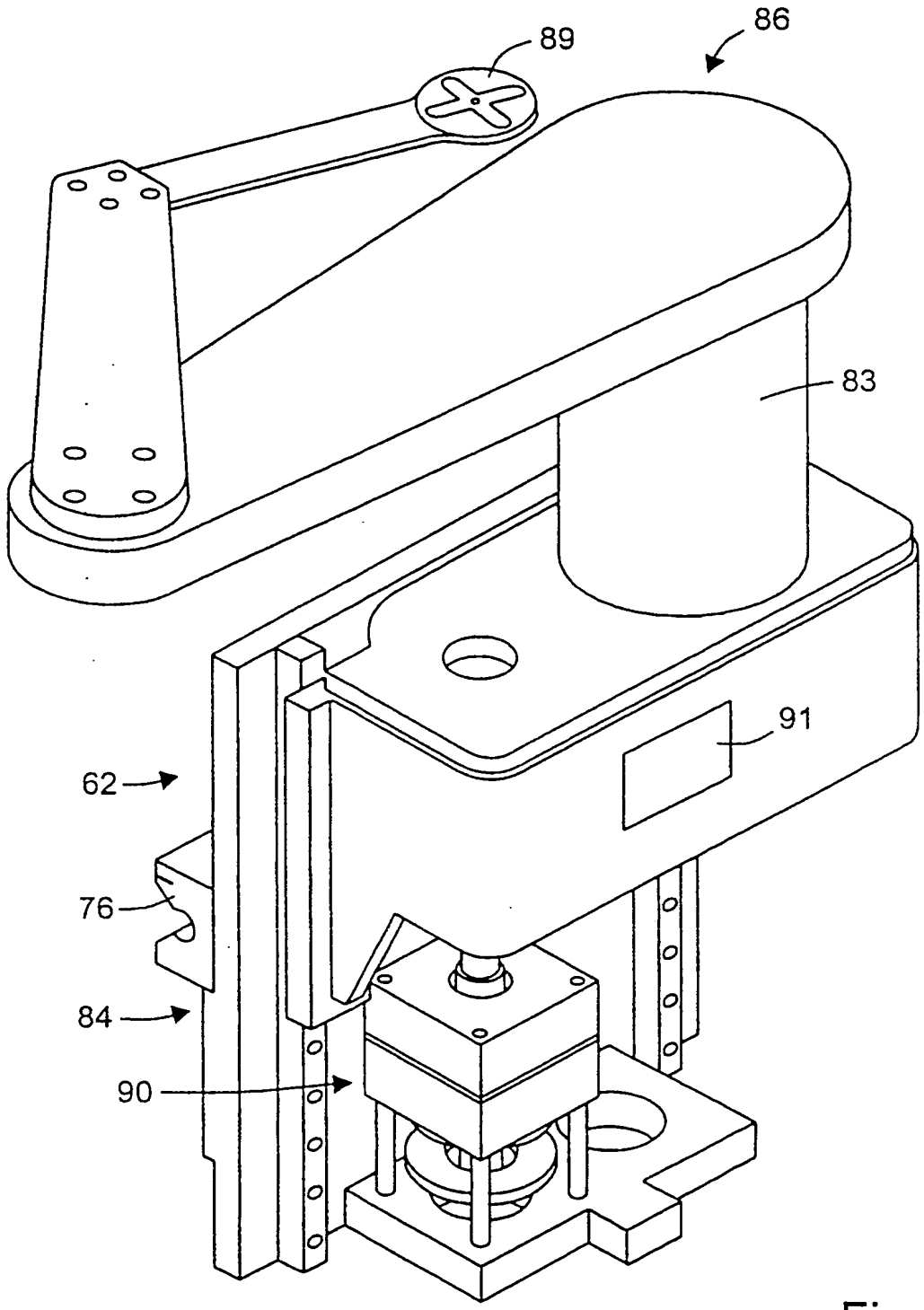


Fig. 19

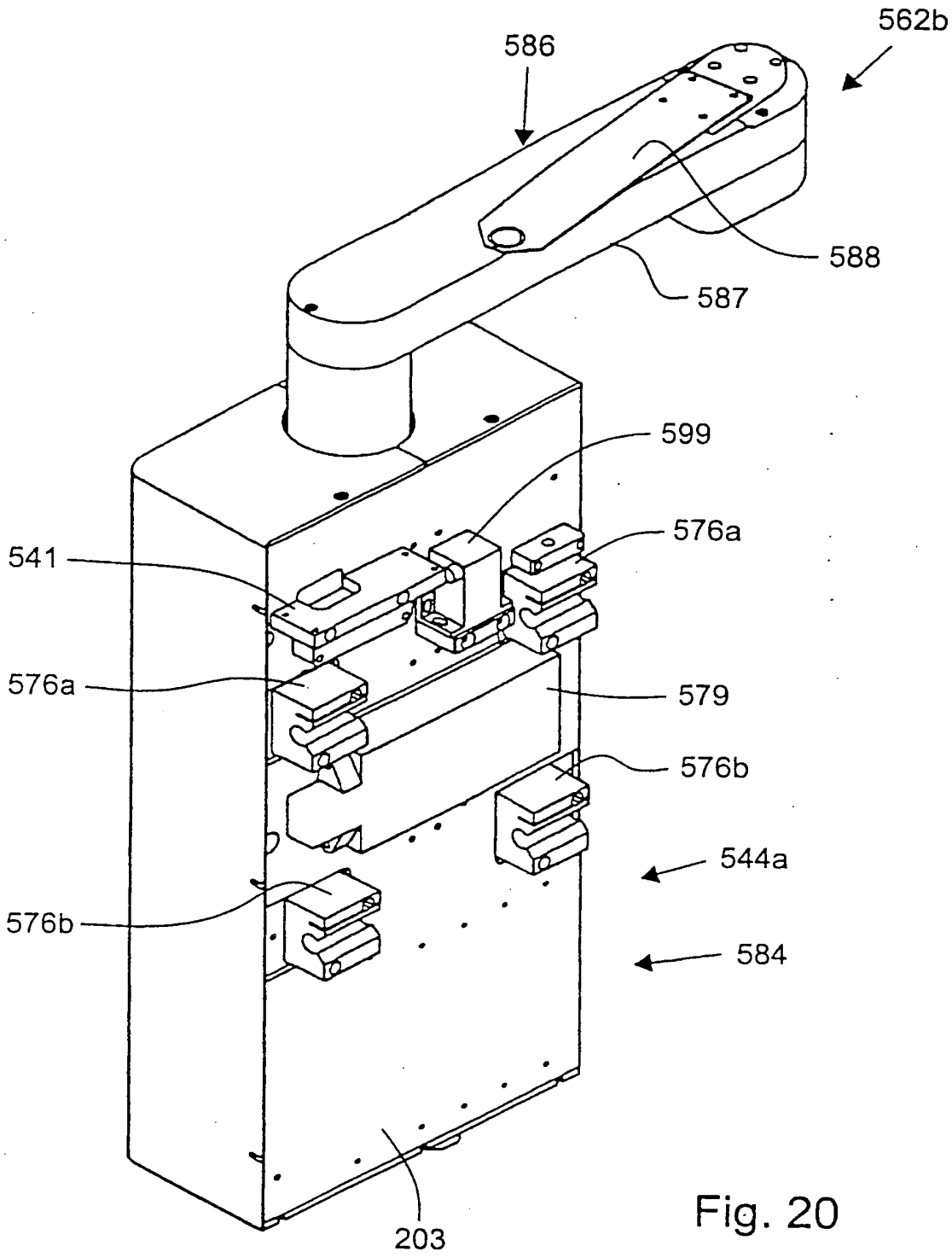
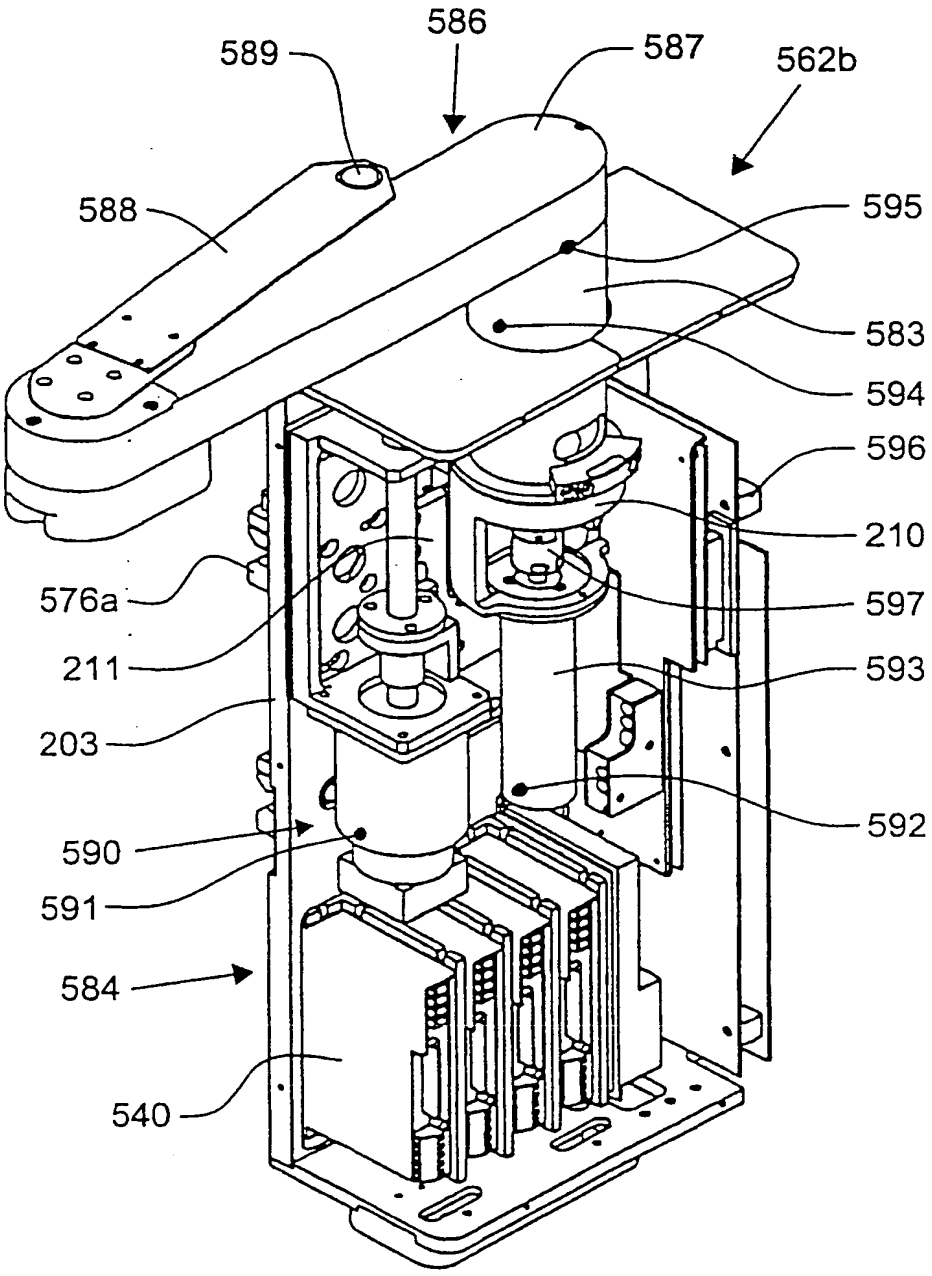


Fig. 20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584
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Fig. 21

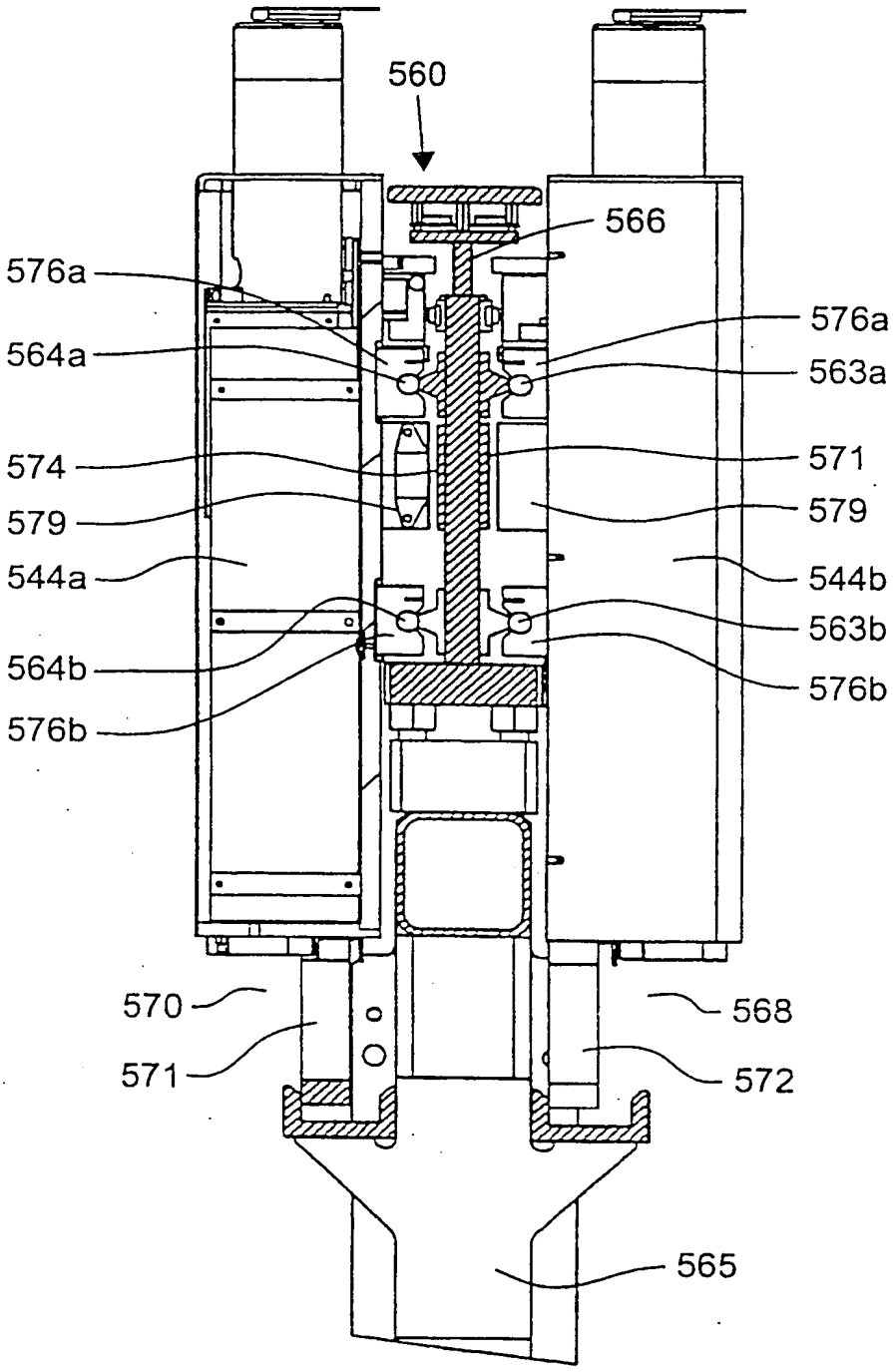
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Fig. 22

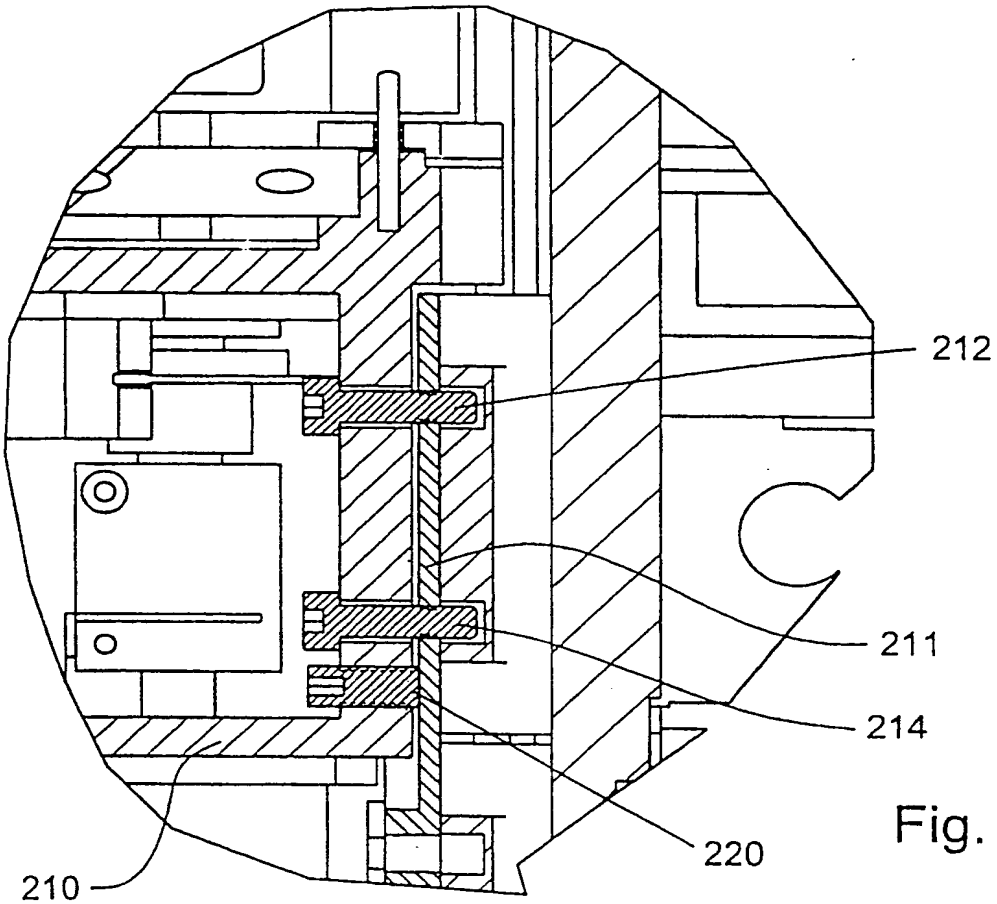


Fig. 23

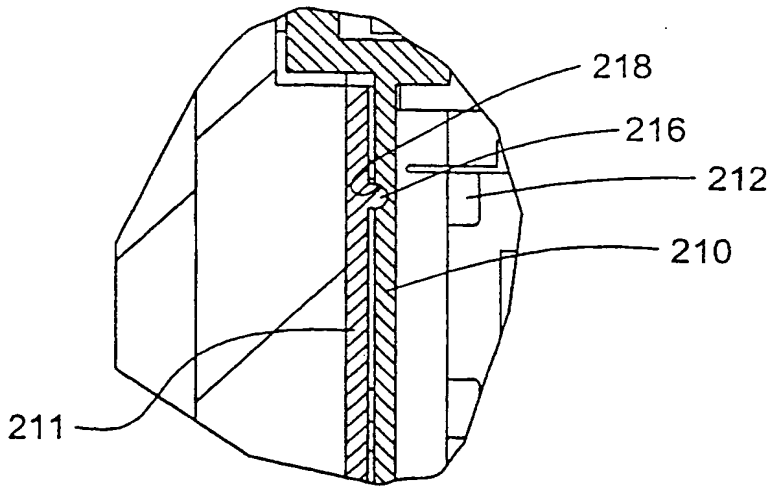


Fig. 24

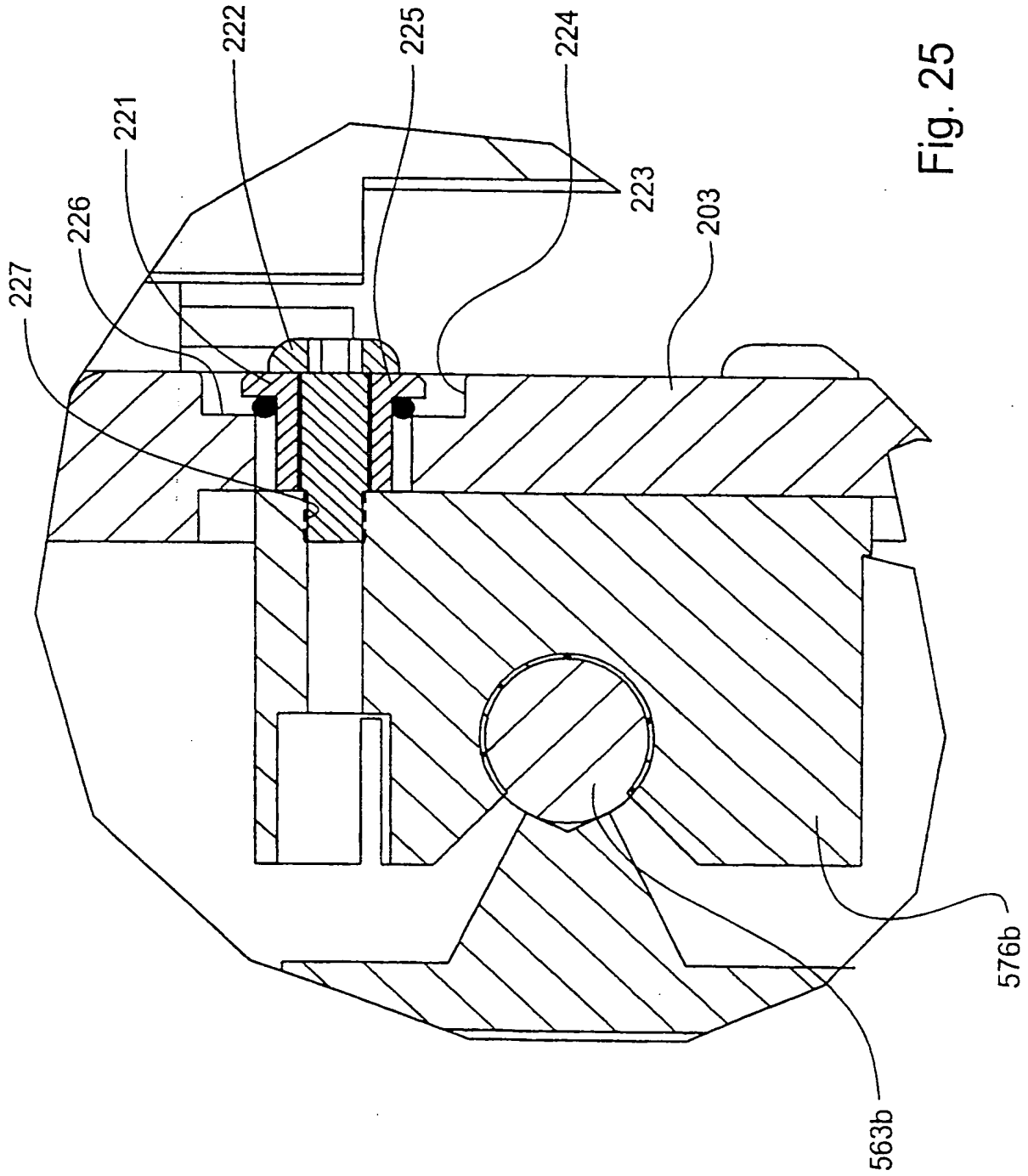
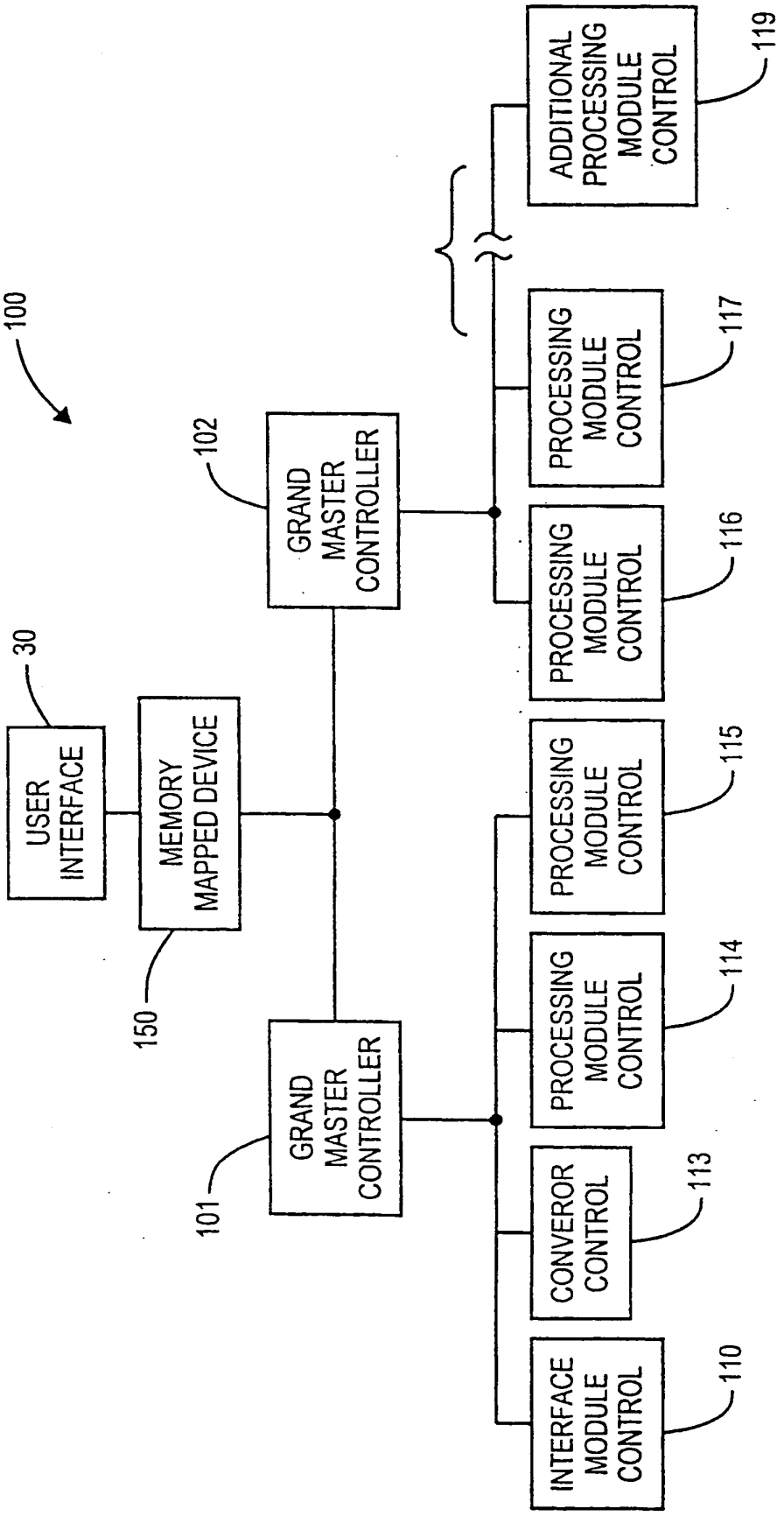


Fig. 25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USER INTERFACE
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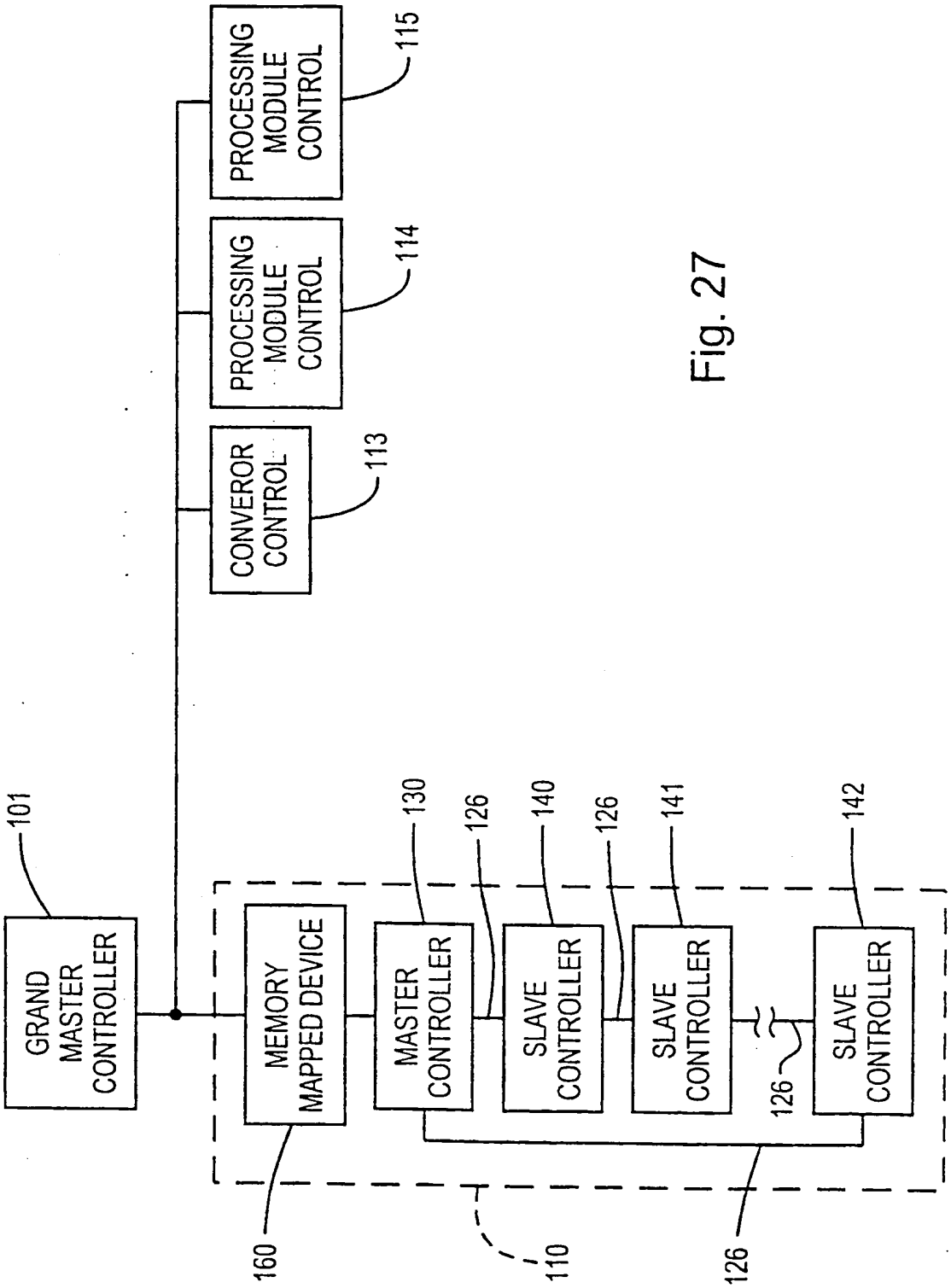
MEMORY MAPPED DEVICE
150
GRAND MASTER CONTROLLER
102
GRAND MASTER CONTROLLER
101
INTERFACE MODULE CONTROL
110
CONVEROR CONTROL
113
PROCESSING MODULE CONTROL
114
PROCESSING MODULE CONTROL
115
PROCESSING MODULE CONTROL
116
PROCESSING MODULE CONTROL
117
ADDITIONAL PROCESSING MODULE CONTROL
119

Fig. 26


PROCESSING MODULE CONTROL
115
PROCESSING MODULE CONTROL
114
CONVEROR CONTROL
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GRAND MASTER CONTROLLER
MEMORY MAPPED DEVICE
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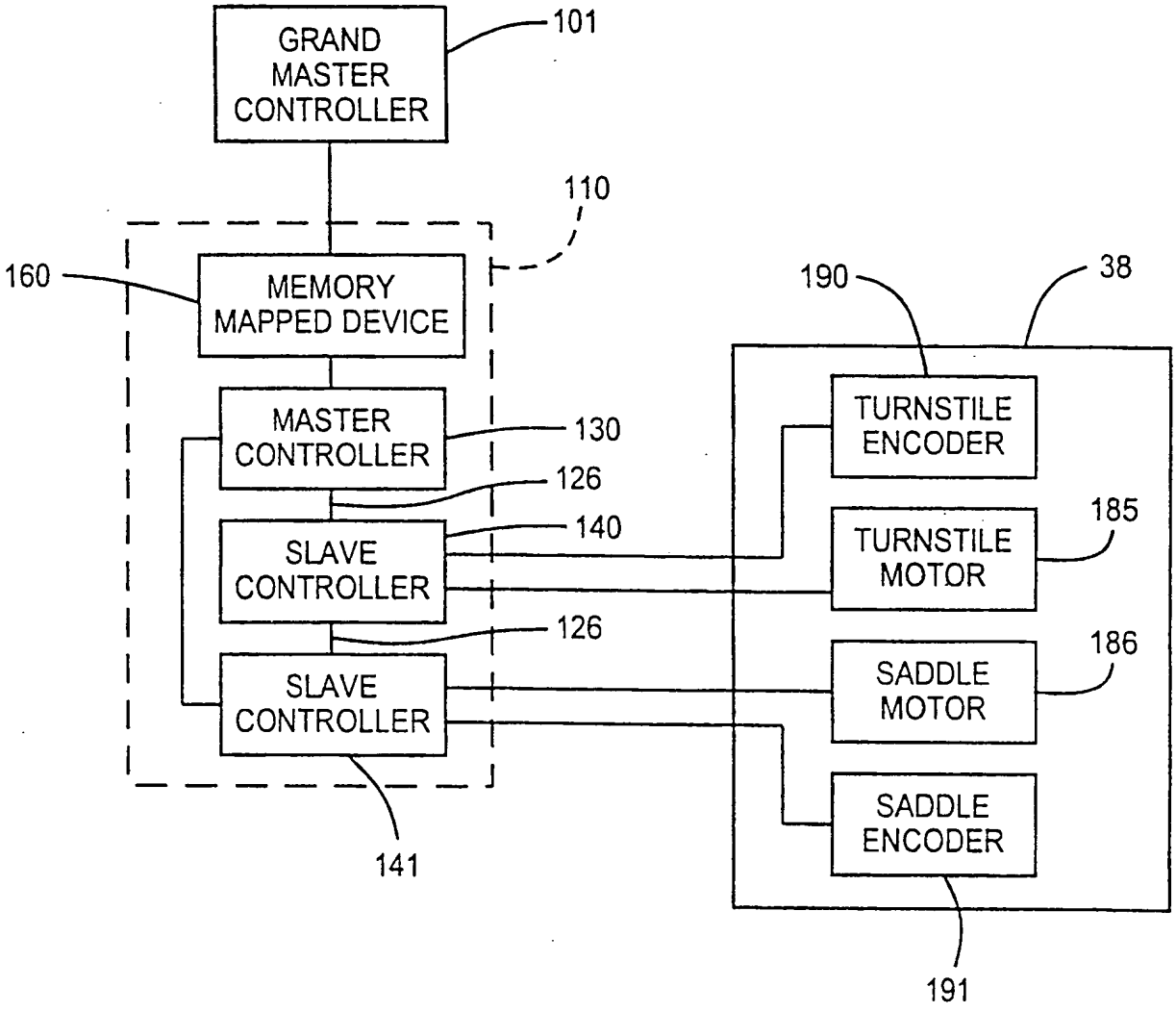
MASTER CONTROLLER
126
140
SLAVE CONTROLLER
126
141
SLAVE CONTROLLER
126
142
SLAVE CONTROLLER
160
110
126

Fig. 27


GRAND MASTER CONTROLLER
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110
160
MEMORY MAPPED DEVICE
MASTER CONTROLLER
130
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SLAVE CONTROLLER
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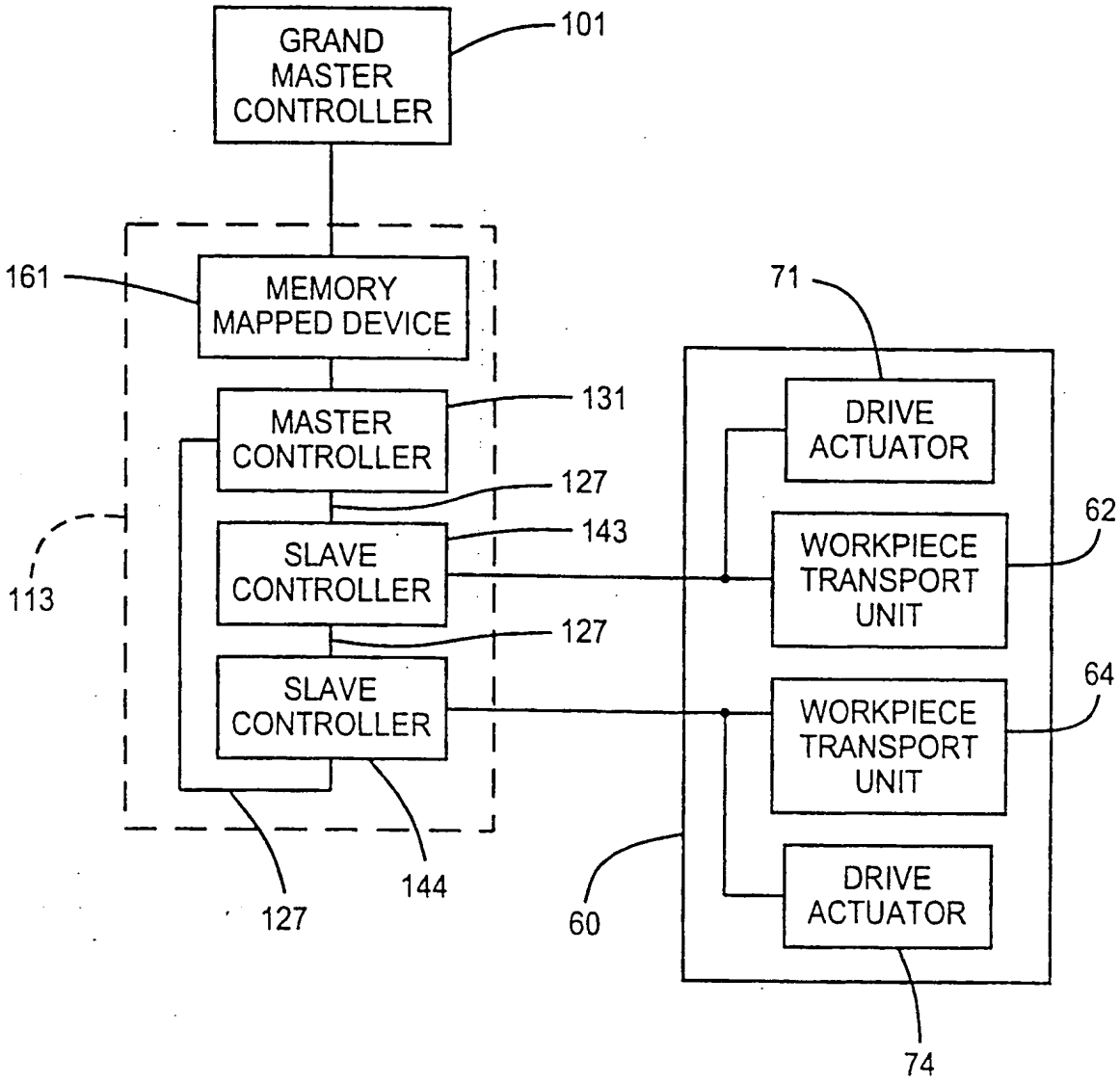
126
SLAVE CONTROLLER
141
190
38
TURNSTILE ENCODER
TURNSTILE MOTOR
185
SADDLE MOTOR
186
SADDLE ENCODER
191

Fig. 28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MEMORY MAPPED DEVICE
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MASTER CONTROLLER
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SLAVE CONTROLLER
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SLAVE CONTROLLER
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144
127
60
71
DRIVE ACTUATOR
62
WORKPIECE TRANSPORT UNIT
64
WORKPIECE TRANSPORT UNIT
DRIVE ACTUATOR
74

Fig. 29

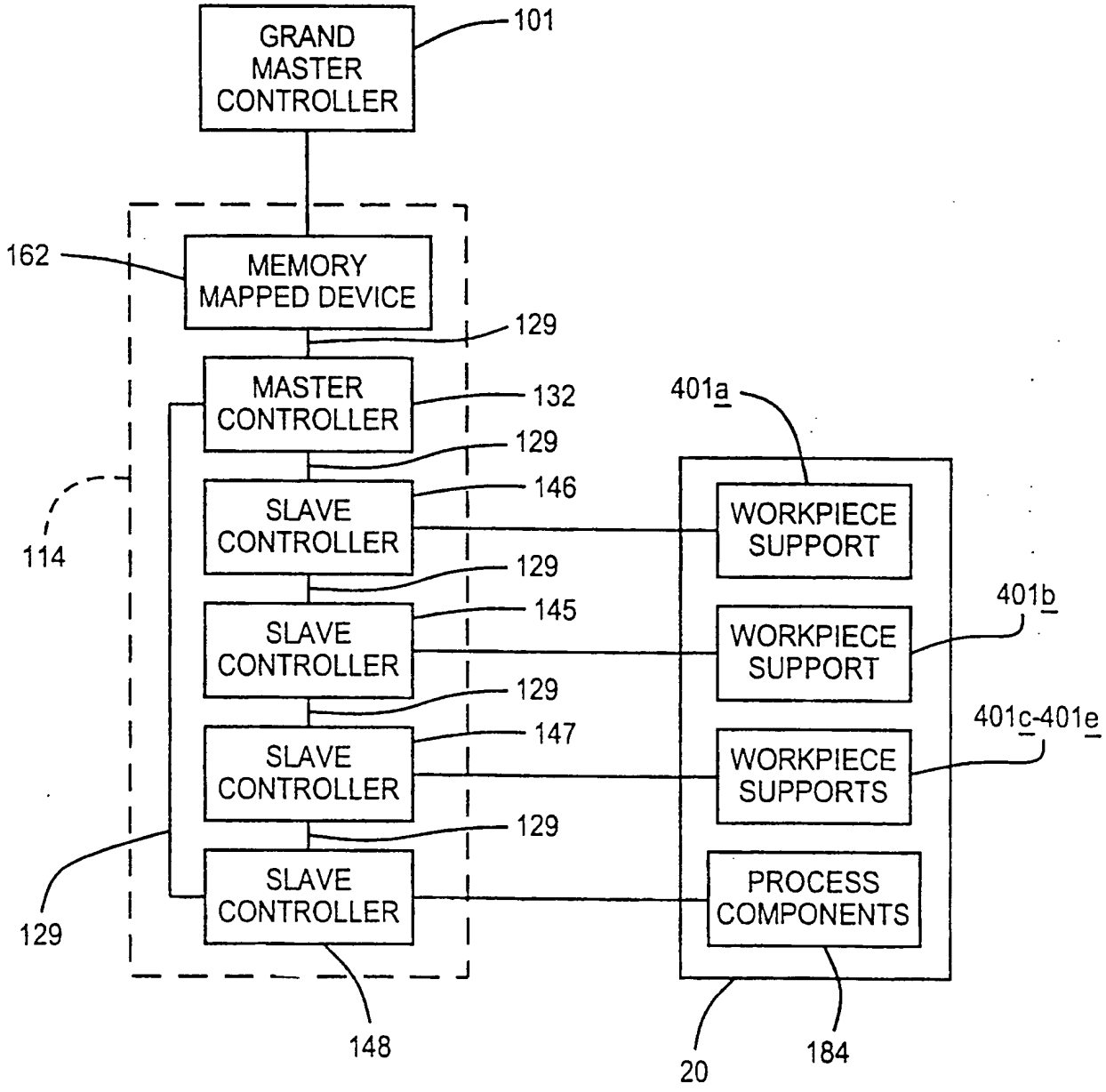

GRAND MASTER CONTROLLER
101
162
MEMORY MAPPED DEVICE
129
MASTER CONTROLLER
132
129
SLAVE CONTROLLER
146
129
SLAVE CONTROLLER
145
129
SLAVE CONTROLLER
147
129
SLAVE CONTROLLER
114
129
148
401a
WORKPIECE SUPPORT
401b
WORKPIECE SUPPORT
401c-401e
WORKPIECE SUPPORTS
PROCESS COMPONENTS
20
184

Fig. 30

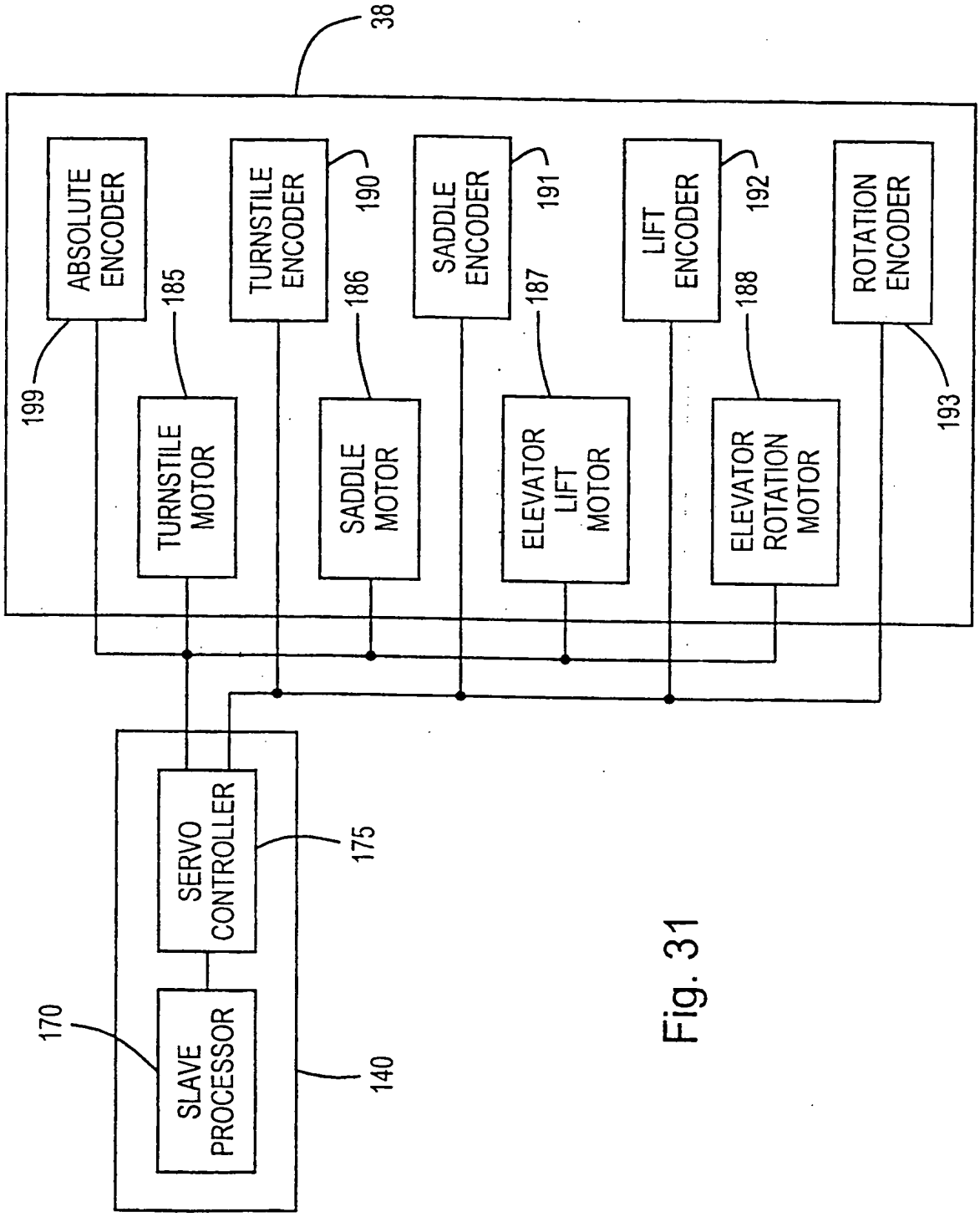

38
ABSOLUTE ENCODER
199
185
TURNSTILE MOTOR
TURNSTILE ENCODER
190
186
SADDLE MOTOR
SADDLE ENCODER
191
187
ELEVATOR LIFT MOTOR
LIFT ENCODER
192
188
ELEVATOR ROTATION MOTOR
ROTATION ENCODER
193
SERVO CONTROLLER
175
SLAVE PROCESSOR
170
140

Fig. 31

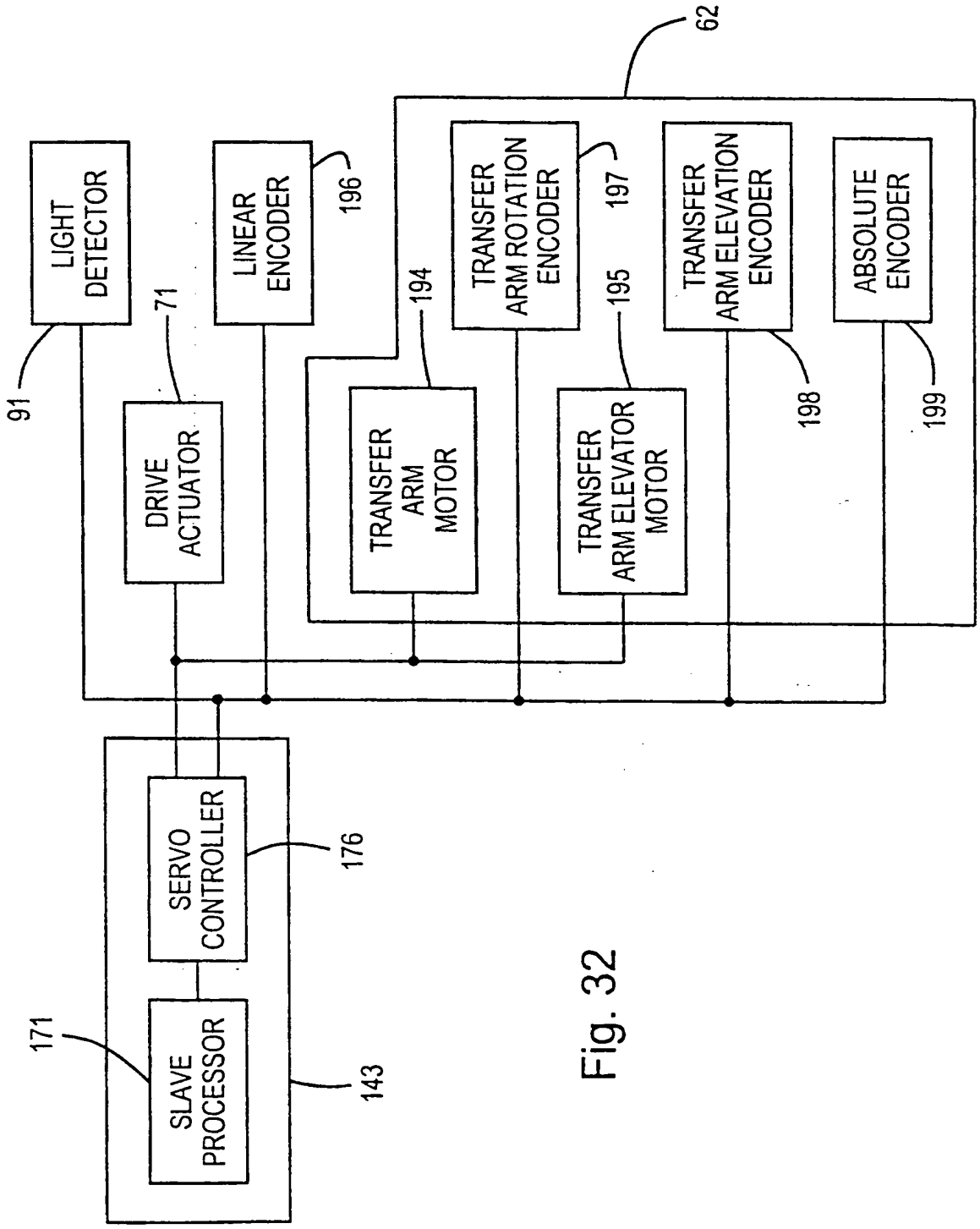
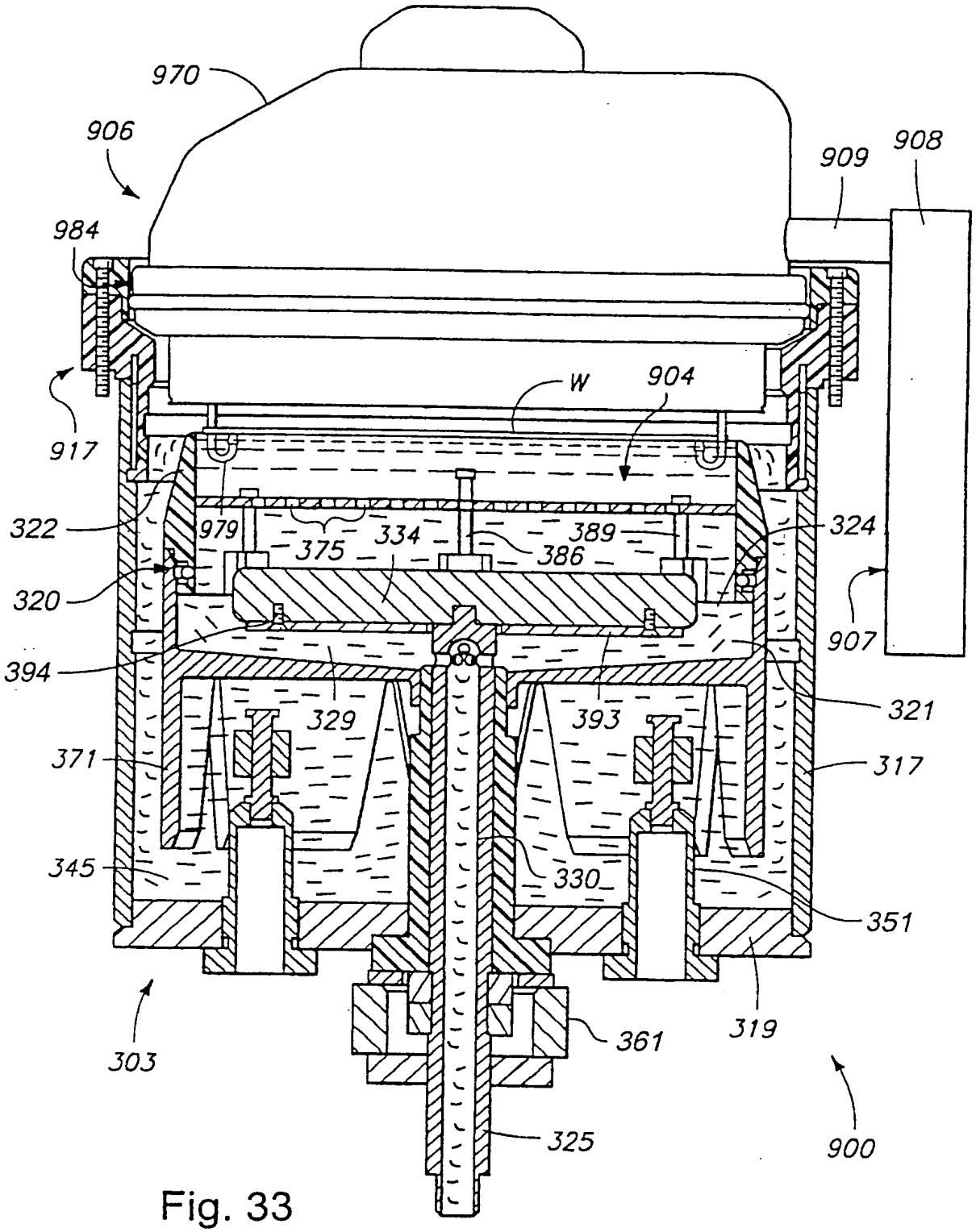

62
LIGHT DETECTOR
91
71
DRIVE ACTUATOR
LINEAR ENCODER
196
194
TRANSFER ARM MOTOR
TRANSFER ARM ROTATION ENCODER
197
195
TRANSFER ARM ELEVATOR MOTOR
TRANSFER ARM ELEVATION ENCODER
198
ABSOLUTE ENCODER
199
SERVO CONTROLLER
176
SLAVE PROCESSOR
171
143

Fig. 32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361
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900

Fig. 33

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/00132

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 21/68; B65G 1/00, 35/00, 37/00, 41/00, 43/00, 49/07
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 29/25.01; 198/301, 340, 341, 358, 464.1, 571, 575, 619; 414/273, 935-941

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

STN
search terms: magnetic#, electromagnetic#, motor#, wafer#, rail?, tram, trams, hanson, kyle, linear

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,660,517 A (THOMPSON et al) 26 August 1978 (26.08.78), column 3, line 19 to column 24, line 4.	1-32
X	US 5,664,337 A (DAVIS et al) 09 September 1997 (09.09.97), column 1, line 10 to column 23, line 67.	1-32
X	US 5,678,320 A (THOMPSON et al) 21 October 1997 (21.10.97), column 1, line 10 to column 28, line 22.	1-32
A	US 5,172,803 A (LEWIN) 22 December 1992 (22.12.92), column 1, lin 61 to column 2, line 19.	1-7, 9, 16, 17, 22, 26-32

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 24 JUNE 1998	Date of mailing of the international search report 29 OCT 1998
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer DAVID E. GRAYBILL Telephone No. (703)308-1778

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/00132

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

29/25.01; 198/301, 340, 341, 358, 464.1, 571, 575, 619; 414/273, 935-941

DOCKET NO: 1999 P 8051

SERIAL NO: _____

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